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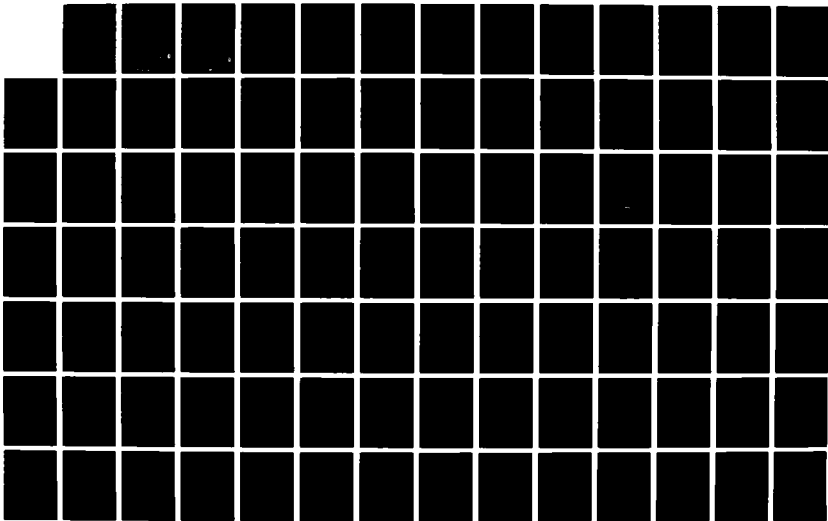
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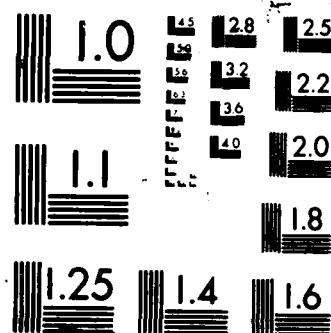
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FABRICATION OF AlGaAs/InGaAs  
PSEUDOMORPHIC MODULATION DOPED  
FIELD EFFECT TRANSISTORS  
WITH P-DOPED SURFACE LAYERS

THESIS

Thomas E. McLaughlin  
First Lieutenant, USAF

AFIT/GE/ENG/86D-11

DEPARTMENT OF THE AIR FORCE  
AIR UNIVERSITY

**AIR FORCE INSTITUTE OF TECHNOLOGY**

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FABRICATION OF AlGaAs/InGaAs PSEUDOMORPHIC MODULATION DOPED  
FIELD EFFECT TRANSISTORS WITH P-DOPED SURFACE LAYERS

THESIS

Presented to the Faculty of the School of Engineering  
of the Air Force Institute of Technology  
Air University  
In Partial Fulfillment of the  
Requirements for the Degree of  
Master of Science in Electrical Engineering



Thomas E. McLaughlin, B.S.E.E.  
First Lieutenant, USAF

December 1986

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## Preface

In this effort, a  $p^+$ -layer was grown on top of pseudomorphic InGaAs/AlGaAs MODFETs. The intent was to show that the concept of Schottky barrier modification, established in earlier research, could be extended to the pseudomorphic MODFET. A great deal of useful information was established about the DC and microwave characteristics of the device, and the lessons learned here should prove valuable in any future efforts to produce enhanced Schottky barriers on MODFET structures.

I am deeply in debt to Dr. Hadis Morkoc, Andrew Ketterson and Tim Henderson of the University of Illinois Coordinated Sciences Laboratory. They provided the MBE-grown material for this effort and aided significantly in the fabrication process. Thanks also go to Joe Grzyb, Mary Harshbarger, Larry Callahan and Robert Neidhard for their help in fabrication and testing at the Air Force Avionics Laboratory, and to G. L. McCoy for his continued support.

Sincere thanks also go to Mr. Cole Litton for his sponsorship of the project and for the innumerable discussions, encouragement and guidance that helped this project reach fruition. The insights and expertise were without parallel. Major Don Kitchen, my thesis advisor, also provided regular guidance and encouragement, and Major Ed Kolesar was a valuable catalyst for ideas.

Most importantly, my thanks to my wife Renee and daughter Michelle for their innumerable sacrifices and encouragement.

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## Abstract

In this investigation, modulation doped field-effect transistors (MODFETs) were fabricated. Two recently developed improvements to the MODFET structure were incorporated to produce an electronic device that had never before been fabricated. Highly p-doped surface layers were incorporated under the gate contact of the device. These layers have been shown to increase the Schottky barrier height at the gate contact on devices known as enhanced Schottky (ES) MODFETs. Pseudomorphic AlGaAs/InGaAs technology was also incorporated for its proven unsurpassed electron saturation velocity and resulting high speed of operation. Those two complementary technologies were combined in this effort to produce the ES pseudomorphic MODFET, to take advantage of fast speed of operation and high Schottky barrier heights.

To evaluate the response of these ES pseudomorphic devices, their characteristics were measured and compared directly with those of reference samples fabricated at the same time from the same substrate material. The p-layers of the reference transistors were etched off chemically just before deposition of gate contact metal. The peak transconductance, threshold voltage, contact resistance and barrier height of all devices were measured at direct current (DC). Also, microwave S-parameters were measured over the range of 2 to 12 gigahertz (GHz), and figures of merit were derived from these measurements.

Qualitatively, the performance of devices fabricated in this effort approached the best reported for devices of this family. These devices exhibited transconductance as high as 230 mS/mm. This value is unsurpassed for devices with the 1.35 - 1.5  $\mu\text{m}$  gate lengths used here. Similarly, the devices were capable of providing gain at frequencies as high as 17.5 GHz. These values also are very high for devices with this gate length. Normalized contact resistances were also measured. The lowest value observed here (0.002  $\Omega\text{-mm}$ ) surpasses the best published value of 0.035  $\Omega\text{-mm}$  for MODFET devices.

Based on calculations using a charge control model developed in an earlier effort, the devices with p-type layers were expected to exhibit higher gate Schottky barrier heights than similar reference samples without p-layers. Unexpectedly, there was no evidence of the enhanced barrier height. Those devices exhibited Schottky barrier heights consistently slightly lower than those of the reference transistors without p-layers, fabricated from the same substrate material. Three different physical phenomena are given as possible explanations for this observation.

The reference transistors similarly exhibited higher transconductance, threshold voltage and microwave response than the samples with p-layers. This observation can be traced to the greater distance between the gate contact and the current conduction channel in the device with the p-layer.

## I. Introduction

### Motivation

From the first transistor, there has been a continuing, comprehensive effort to develop transistors that are faster, more efficient, more reliable and smaller in size. Modulation-doped field-effect transistors (MODFETs), also known as high electron mobility transistors (HEMTs) and two-dimensional electron gas field-effect transistors (TEGFETs), are one of the latest evolutionary steps in the development cycle. MODFETs, like metal-semiconductor transistors (MESFETs), have a Schottky barrier gate which controls current between source and drain contacts (Fig 1).

However, the novel structure of a MODFET allows for fast operation, surpassing MESFET capability in microwave frequency operation. This feature is a result of the unique properties of the n-type AlGaAs and intrinsic GaAs heterojunction, where charge carrying electrons are confined to a thin, very high mobility quantum well. The MODFET is the fastest commercially available transistor in the world (1), and is second only to the Josephson junction as the fastest operating semiconductor device yet to be realized (2:30).

One critical problem with the MODFET is its inability to support gate voltages larger than the gate barrier height without incurring significant amounts of leakage current. A recent modification to the MODFET structure involves the addition of a thin  $p^+$ -layer beneath the transistor gate



Schottky barrier contact. This modified device is known as an enhanced Schottky (ES) MODFET. The  $p^+$ -layer alters the gate barrier height, allowing larger voltages to be impressed on the gate. As a result, the addition of this layer has allowed the barrier height to increase from 0.8 eV in the standard MODFET to as high as 1.6 eV (3:1-2). While the ES MODFET allows higher gate voltages, microwave performance, power handling capability and noise immunity of this modified structure have yet to be measured and analyzed.

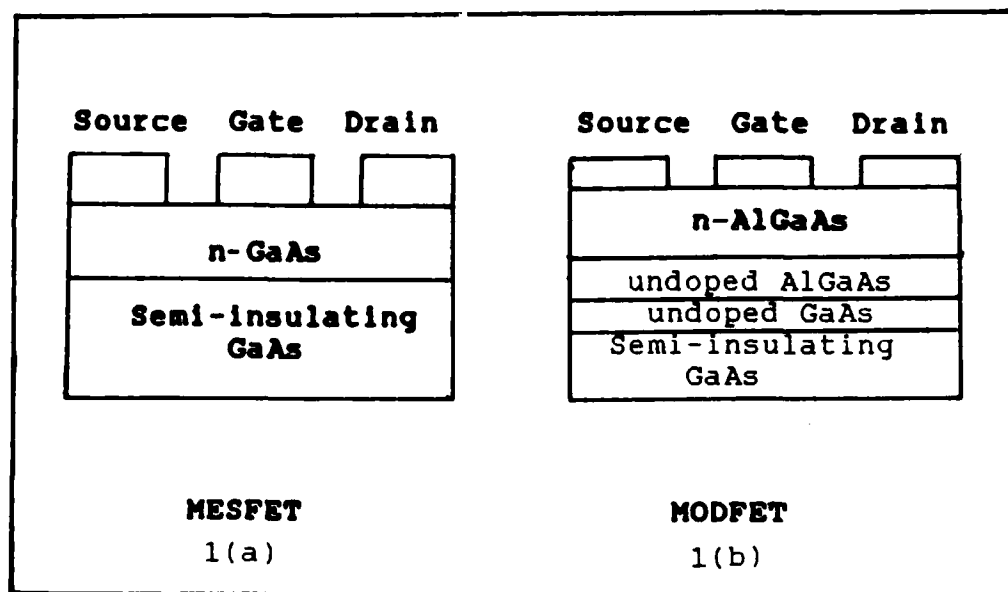


Fig 1. MESFET and MODFET Structures (3:1-2).

The high electron mobility of the MODFET was first demonstrated in 1978 (2:28). The MODFET with GaAs and AlGaAs layers was the first used and has been the most widely studied. Recently, however, experiments have been undertaken with new materials in anticipation of improving

device characteristics. Notable among these are InP/InGaAs (4) and AlInAs/InGaAs (5). Another variation uses the InGaAs/AlGaAs system (Fig 2). This device is known as a "pseudomorphic" MODFET because of the crystal structure at the InGaAs-AlGaAs interface (6:564). This structure has improved high frequency performance over the standard MODFET of Fig 1(b). This feature is a result of a higher electron saturated drift velocity in InGaAs compared to GaAs (6:564), and to the improved charge carrier (electron) confinement in the quantum well of the pseudomorphic device. The quantum well in this device is approximately twice as large as that of the standard AlGaAs/GaAs device. The placement of highly doped  $p^+$ -layers on this device to enhance the barrier has yet to be accomplished.

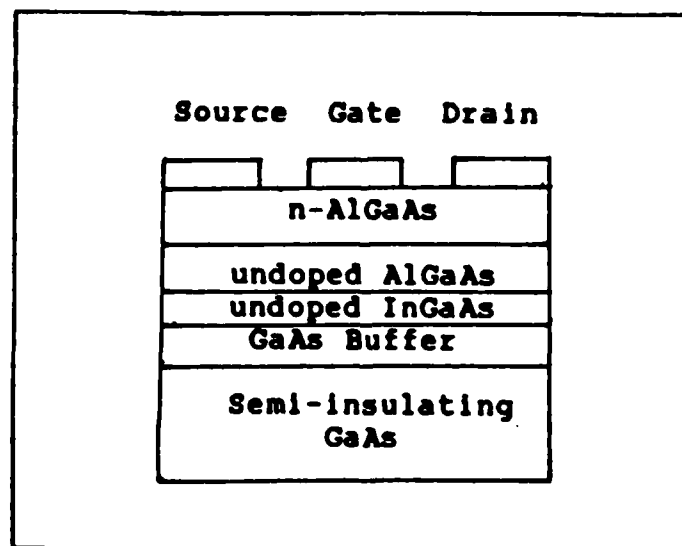


Fig 2. Pseudomorphic InGaAs/AlGaAs MODFET.

## Problem

The concept of modifying gate barrier heights through the use of doped semiconductors was postulated by Shannon (7) and first applied by Eglash, Newman, Pan, Spicer, Collins, and Zurakowski (8). Priddy (3) has shown that the concept can be applied to AlGaAs/GaAs MODFETs, and the gate barrier height raised significantly with a thin  $p^+$ -layer. Ohata, Hida and Miyamoto (9) have shown that the structure exhibits a high direct current (DC) transconductance, as well as a low noise figure and high gain at radio frequencies (RF). Hida, Ohata, Suzuki and Toyoshima (10) have shown that a similar structure with an undoped GaAs layer under the gate also exhibits high DC and RF performance. Since improved performance at high frequencies is an ultimate goal, it is only logical to extend the barrier modification concept to the higher frequency-operating pseudomorphic MODFETs.

The problem then is to extend the concept of barrier enhancement to pseudomorphic MODFETs. GaAs layers doped with Be will be fabricated under the gate contact on pseudomorphic MODFETs. The DC and microwave performance of these devices will also be measured and compared to reference devices without  $p^+$ -layers. The anticipated result is improved noise performance at higher frequencies without an accompanying sacrifice in the device's current gain. Accordingly, the improved performance may then be quantified, and

its impact for Air Force electronic systems estimated.

### Scope

The purpose of this thesis is to fabricate, characterize and analyze the high frequency response of the pseudomorphic ES MODFET. DC and high frequency performance measurements will be made. The responses of the ES pseudomorphic MODFET with a  $p^+$ -cap will be compared to similar (control) devices without  $p^+$ -layers, made from the same wafer. No refinement of the theory developed for ES MODFETs will be undertaken.

### Major Results

Pseudomorphic MODFETs with  $p^+$ -layers were successfully fabricated. The resultant barrier characteristics were not as expected. Instead of enhancing the barrier, the  $p^+$ -layer consistently produced slightly lower gate Schottky barriers. This result may be attributed to one of two causes.

The very high doping of the  $p^+$ -layer may have been beyond the saturation limit. This would result in precipitation of Be dopant atoms at the GaAs/AlGaAs interface, altering band structure and lowering the barrier.

A second possibility is that the band structure of the pseudomorphic MODFET is sufficiently different from the standard MODFET that the theory developed by Priddy (3) does not accurately predict the behavior of this device. The  $p^+$ -layer could itself cause undesired band bending, resulting in the lower barrier.

The control samples exhibited higher threshold voltage, transconductance and microwave response as compared to the devices with  $p^+$ -layers. These results are a consequence of the smaller distance between the gate contact and the conducting channel in the control sample.

### Sequence of Presentation

Chapter II summarizes the critical elements of the MODFET theory. It describes the basic principles of the MODFET, and highlights the needs that motivated the development of the ES MODFET and the pseudomorphic MODFET. These new structures and rationale for developing a pseudomorphic MODFET with a  $p^+$ -layer are described. Parameters that describe the high frequency behavior of these different devices are also discussed. Chapter III describes the equipment used to fabricate and evaluate MODFET devices. Chapter IV discusses the fabrication, experimental instrumentation arrangement and procedures implemented to evaluate device performance. The experimental results are also presented. Chapter V analyzes the results of this procedure. Conclusions and recommendations for future study of these devices are noted in Chapter VI.

## II. Theoretical Development

In this thesis effort, the high frequency performance of certain MODFET structures are measured and compared. It is necessary to first describe the basic MODFET and the rationale for varying the structure to improve performance. The criteria for quantifying that improvement must be defined. The basic principles of the MODFET will be noted, including its fabrication, principles of charge transport, and modes of operation. The ES and pseudomorphic MODFETs will be introduced as solutions to certain limitations of the standard device. The integration of those complementary technologies to produce a higher performance device will be introduced. Finally, the parameters to measure that performance at microwave frequencies will be discussed.

In conventional MESFETs, electron donors incorporated into the semiconductor material provide charge carrying electrons. These electrons carry charge through the active regions of the device. Naturally, with higher impurity concentrations in a material, more electrons should be available to carry current, and the device can be switched on and off faster, as a result. However, higher doping means that there are more atoms with which the free electrons may interact via their coulombic potentials (11:774). Ionized impurity scattering is one mechanism which decreases the efficiency of electrons in carrying charge through a

transistor, and is the dominant mobility-limiting mechanism at low temperatures. This decreases the mobility of primary charge carriers (electrons in this case) in the active region of the device (12:1015). This parasitic mechanism is circumvented with the unique structure of MODFETs. The electrons are delocalized from their donor atoms.

### MODFETs

In these devices, electrons are donated by impurities in n-doped  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ , where  $x$  is the mole fraction of Al (Fig 3). These electrons diffuse to and are transported through the undoped GaAs layer. There they exhibit very high saturation velocities. As a result, MODFETs can be switched on or off in less than 10 picoseconds ( $10^{-11}$  seconds) (2:28). The devices provide current amplification at frequencies as high as 70 gigahertz with a 0.25  $\mu\text{m}$  gate length (13:142).

To amplify on MODFET characteristics, it is necessary to first discuss the structure and fabrication of the device.

Structure and Fabrication. MODFET fabrication requires two distinct processing steps. First, the GaAs and AlGaAs crystal layers of the structure are grown on a chromium-doped, semi-insulating GaAs substrate. This is achieved using a thin-film growth technique, such as molecular beam epitaxy. Second, individual MODFETs are then defined on the grown material using standard fabrication techniques.

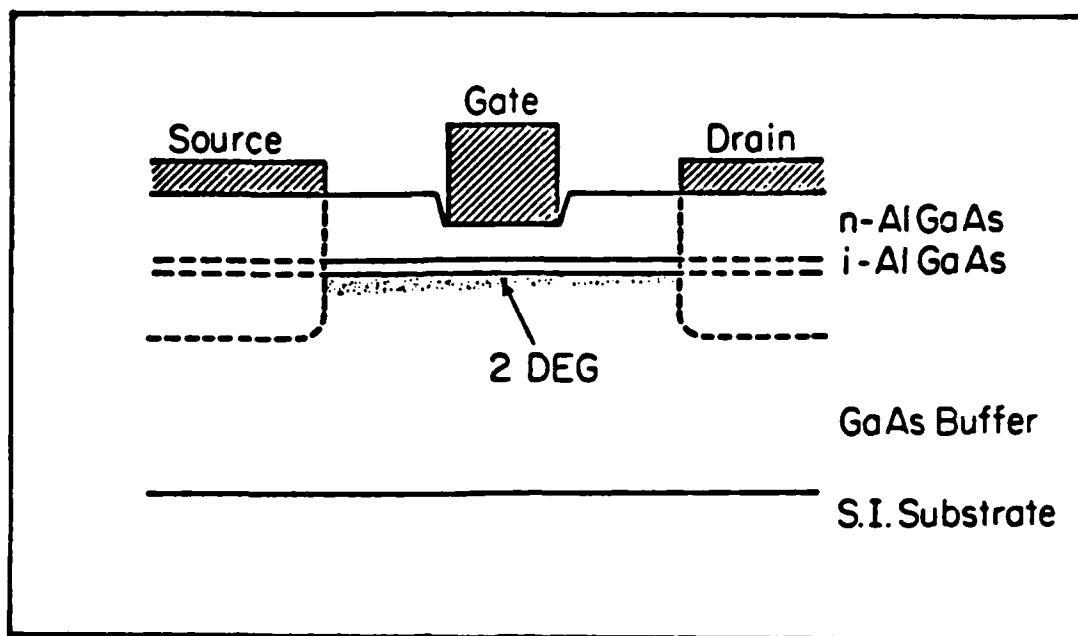


Fig 3. Cross-Sectional View of a MODFET (14).

Molecular Beam Epitaxy (MBE). The AlGaAs and undoped GaAs layers of the MODFET are grown by MBE on semi-insulating GaAs substrates, as indicated in Fig 3. The process is similar to that used for MBE-grown MESFETs. A nominal 1  $\mu\text{m}$  thick GaAs layer, the buffer layer, is grown at a substrate temperature of 580° C (12:1018). This provides a high quality, defect-free interface on which the next layers of material are grown (14:22). An intrinsic AlGaAs layer, called the separation or setback layer, is grown next. It is typically 20-60 Å thick. It is followed by an n-type layer, 300-600 Å thick, also of AlGaAs. This n-AlGaAs layer is nominally silicon-doped to  $2 \times 10^{18} \text{ cm}^{-3}$  (15:118). There may be a GaAs cap layer grown on the AlGaAs to facilitate ohmic contact at the drain and source. Alternately, the n-AlGaAs may be graded down to GaAs near the surface.



Field Effect Transistor (FET) Fabrication. After MBE growth, individual FETs are fabricated from the MBE-grown epitaxial layers. Standard optical lithography techniques are normally used. However, the fabrication of sub-micron geometry FETs requires electron beam lithography.

FET fabrication requires several steps. First, individual devices are isolated in the crystal. Ohmic source and drain contacts are then formed, followed by the metallization of a Schottky barrier-gate. The process is illustrated in Fig 4.

The individual MODFET structures are isolated by chemically etching to the semi-insulating GaAs layer, leaving mesas of active material separated by non-conducting regions. An etchant containing hydrofluoric acid, hydrogen peroxide, and deionized water is commonly used. Alternatively, isolating implants may also be used.

Source and drain contacts are formed next. Typically, AuGe, Ni, and Au layers are evaporated onto the device. These metals are evaporated onto the wafer, either thermally or with an electron gun. Following metallization, the contacts are made ohmic by alloying for a short time (30-60 sec) at 400-500° C. This facilitates the diffusion of Ge into the active layers, past the AlGaAs/GaAs heterointerface, and contact with the GaAs buffer layer (14:53). The result is a high ohmic, n-type region under the source and drain contacts.

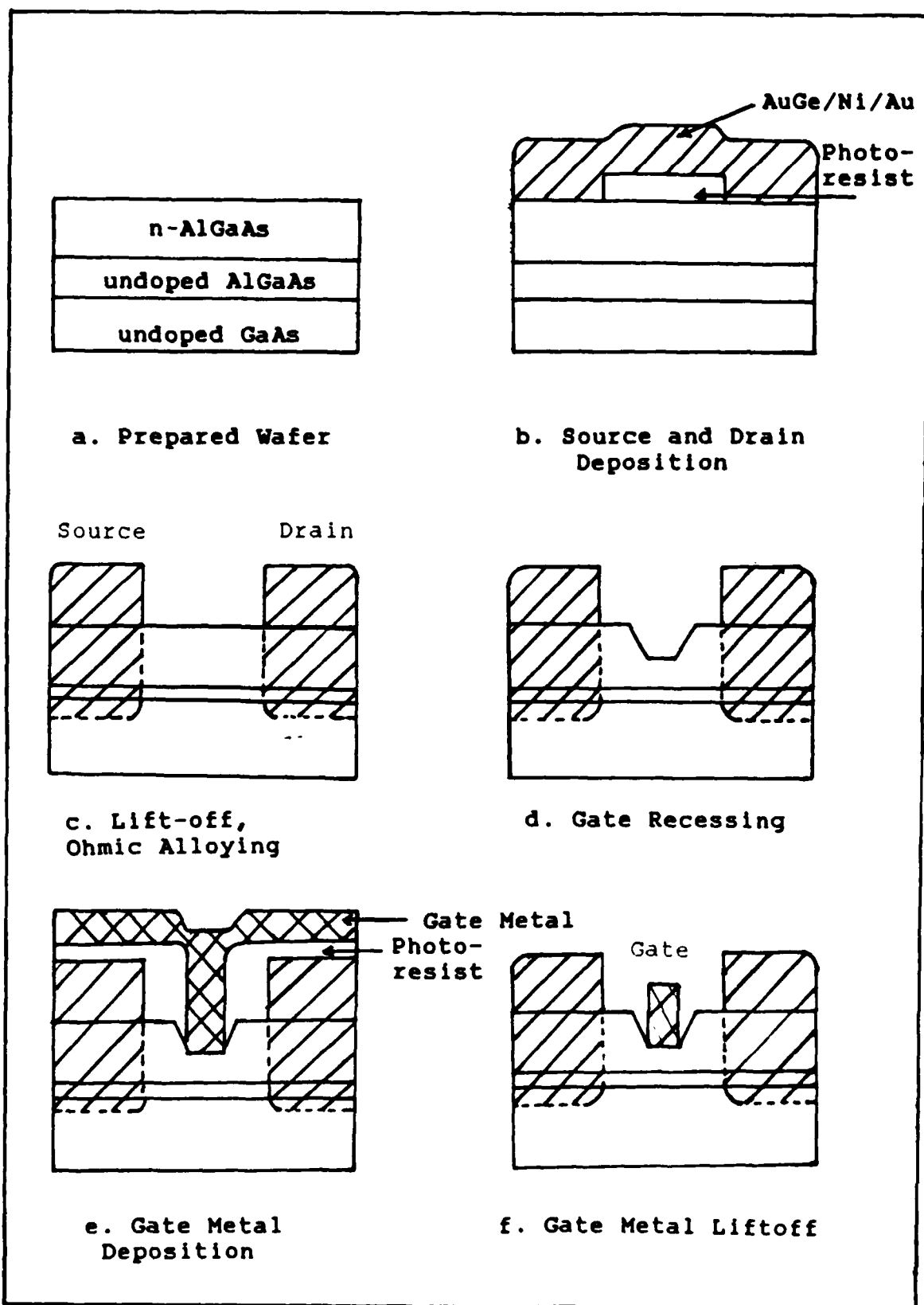


Fig 4. Fabrication Process for MODFET.

The Schottky barrier-gate is formed next. Often, the material under the gate region is partially etched to place the gate contact closer to the AlGaAs-GaAs interface. Reccessing is performed by chemical etching, reactive ion etching, or ion milling. This recessment places the gate contact very close to the GaAs buffer layer and facilitates improved transistor control via the gate Schottky barrier. The gate is finally metallized. The gate metal is chosen for its ability to adhere to the AlGaAs and for the Schottky barrier height it produces. It is often Al or a Ti and Au combination.

A completely fabricated MODFET consists of active regions of AlGaAs and GaAs on a semi-insulating GaAs substrate. Atop these active regions are the source, gate and drain contacts. Under applied bias, current flows between drain and source contacts. A bias voltage applied to the gate modulates this current.

Principles of Operation. As a heterojunction structure, MODFETs operate as a consequence of the unique properties of the interface between GaAs and AlGaAs. To understand MODFET operation, the energy diagrams that result from the heterojunction must be examined. The two-dimensional electron gas (2DEG) that forms at the AlGaAs/GaAs interface may then be understood. It will be shown that the Schottky barrier gate controls charge in the 2DEG, and the electrical characteristics of the gate determine whether the device operates in enhancement or depletion mode.

Energy Bands. As shown in Fig 5, AlGaAs is a wide bandgap material, while GaAs has a relatively narrow gap. When n-AlGaAs and intrinsic GaAs are joined at a junction as shown in Fig 6, their Fermi energy levels ( $E_f$ ) must line up. Valence bands ( $E_v$ ) and conduction bands ( $E_c$ ) in the two materials must therefore bend.

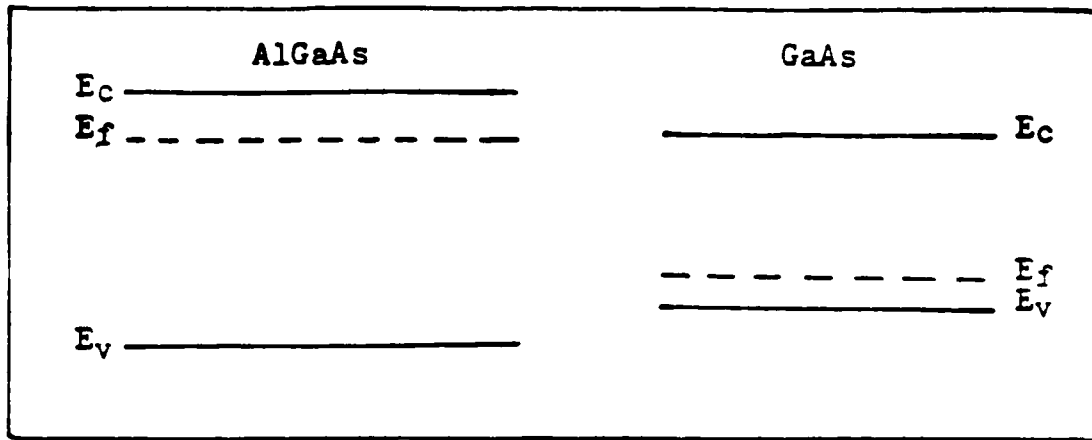


Fig 5. Bandgaps of AlGaAs and GaAs (3:2-7).

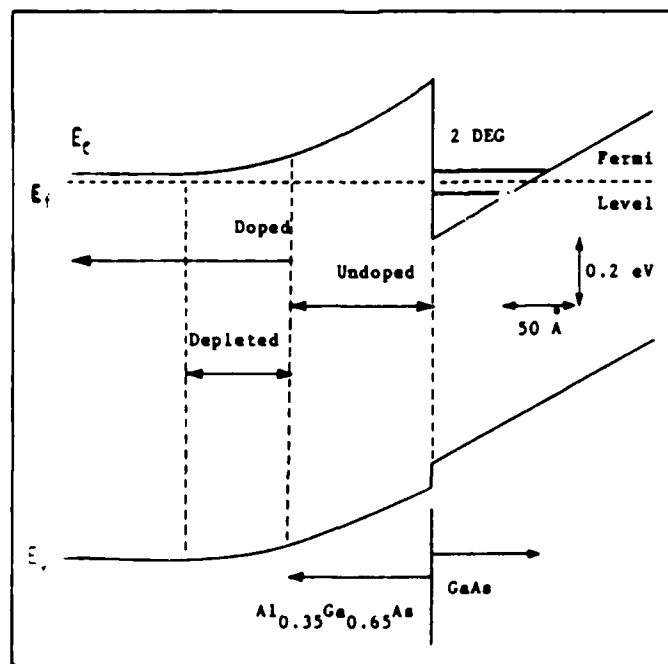


Fig 6. Energy Band Diagram of an AlGaAs/GaAs Heterojunction (3:2-9).

To establish the same  $E_F$  in both materials, electrons in n-AlGaAs must diffuse to the GaAs. This depletes charge from the n-AlGaAs, and the bands bend due to the charge separation. A conduction band discontinuity,  $\Delta E_c$ , due to the difference in bandgaps, causes a potential barrier that prevents electrons from returning to the AlGaAs. As a result, electrons are separated from their donor atoms and trapped in the triangular potential well in GaAs (Fig 6). At room temperature and below, electrons do not have enough thermal energy to overcome the barrier. Obviously at lower temperatures, the carriers in the quantum well are well-confined. The undoped AlGaAs layer shown in Fig 6 is inserted to spatially separate the donated electrons from their donor atoms (16:691). That lowers coulombic interaction and increases transconductance (17).

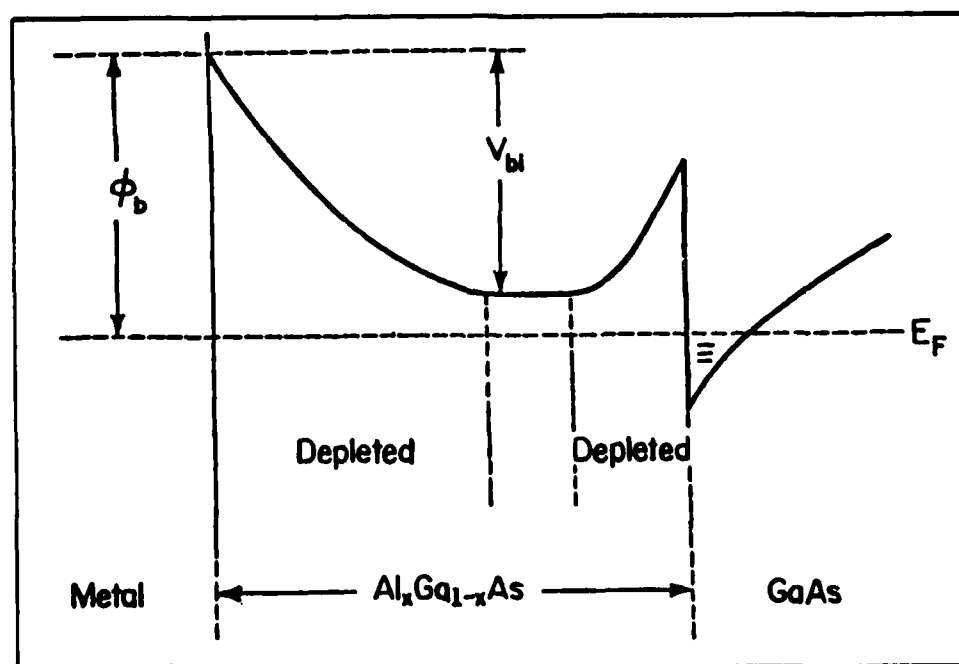


Fig 7. Conduction Band Diagram for a MODFET with Gate Contact (3:2-9).

With a gate contact added, the energy band diagram takes the form shown in Fig 7. The gate contact causes further bending in the AlGaAs, due to the potential of the Schottky barrier,  $\phi_b$ , and charge depletion. Negative applied gate voltage causes further bending, while positive bias decreases the barrier (18:1020).

Two Dimensional Electron Gas. As mentioned, electrons are trapped in a triangular potential well in GaAs near the heterojunction. The well is approximately 100 Å thick (19:705). Electrons cannot return to the AlGaAs because of the barrier, but are free to move along the heterointerface. Ionized impurity scattering does not hinder this motion, because of the very low impurity concentration in intrinsic GaAs. Thus the carriers have a high mobility in their quasi-2DEG confinement. The 2DEG name arises from the fact that electrons move unrestricted along the length and width of the heterojunction. The thickness of the electron gas is very small (10-100 Å) in comparison to the typically 1 µm gate length and 20-300 µm gate width.

Modes of Operation. The gate Schottky barrier, placed on the doped AlGaAs layer, controls the charge and current in the 2DEG in the MODFET "channel". The doped AlGaAs is depleted of electrons at the AlGaAs-GaAs interface by electrons diffusing into GaAs, but this is limited to about 100 Å for  $10^{18} \text{ cm}^{-3}$  doping in the AlGaAs layer (12:1019). The Schottky barrier built-in voltage also depletes charge from

the metal-AlGaAs surface. By comparing Fig 1(a) and (b), it is evident that a parasitic MESFET path exists in the AlGaAs layer, just as in the GaAs channel of the MESFET (17). To avoid conduction in this path, it is necessary to choose parameters such that the AlGaAs-GaAs interface and AlGaAs-metal surface depletion regions just overlap, depleting charge in the n-AlGaAs. This is the reason for recessing the gate during fabrication. It places the gate sufficiently close to the GaAs layer and causes depletion regions to overlap, eliminating conduction in the MESFET.

The resultant operation of a MODFET is similar to that of a MESFET: the Schottky barrier gate voltage controls the number of electrons in the 2DEG by raising or lowering the interface barrier. The number of electrons in the 2DEG determine the amount of current that flows from the source to drain. This relationship can be stated (20:208):

$$n_s = \epsilon_2 (V_g - V_{off}) / q(d + \Delta d) \text{ (cm}^{-3}\text{)} \quad (1)$$

$n_s$  = charge concentration in 2DEG, for  $V_g > V_{off}$

$\epsilon_2$  = dielectric constant in AlGaAs ( $\text{F/cm}^2$ )

$q$  = electronic charge (C)

$d$  = total thickness of AlGaAs beneath gate (see Fig 8)

$d = d_d + d_i$  (Å)

$d_d$  = thickness of n-doped AlGaAs (Å)

$d_i$  = thickness of intrinsic AlGaAs (buffer layer) (Å)

$\Delta d$  = average effective displacement of 2DEG in the GaAs from the heterointerface (Å) (21:1400)

$V_g$  = gate voltage (V)

$V_{\text{off}}$  = threshold voltage; minimum gate voltage for charge concentration (V)

$$V_{\text{off}} = \phi_b - \Delta E_c - V_{p2} \quad (2)$$

(neglecting temperature dependence of Fermi level)

$\phi_b$  = Schottky barrier height (eV)

$\Delta E_c$  = conduction band discontinuity at heterojunction (eV)

$$V_{p2} = qN_d d_d^2 / 2\epsilon_2 \quad (3)$$

$N_d$  = carrier concentration in AlGaAs ( $\text{cm}^{-3}$ )

$d_d$  = thickness of doped AlGaAs beneath gate (Å).

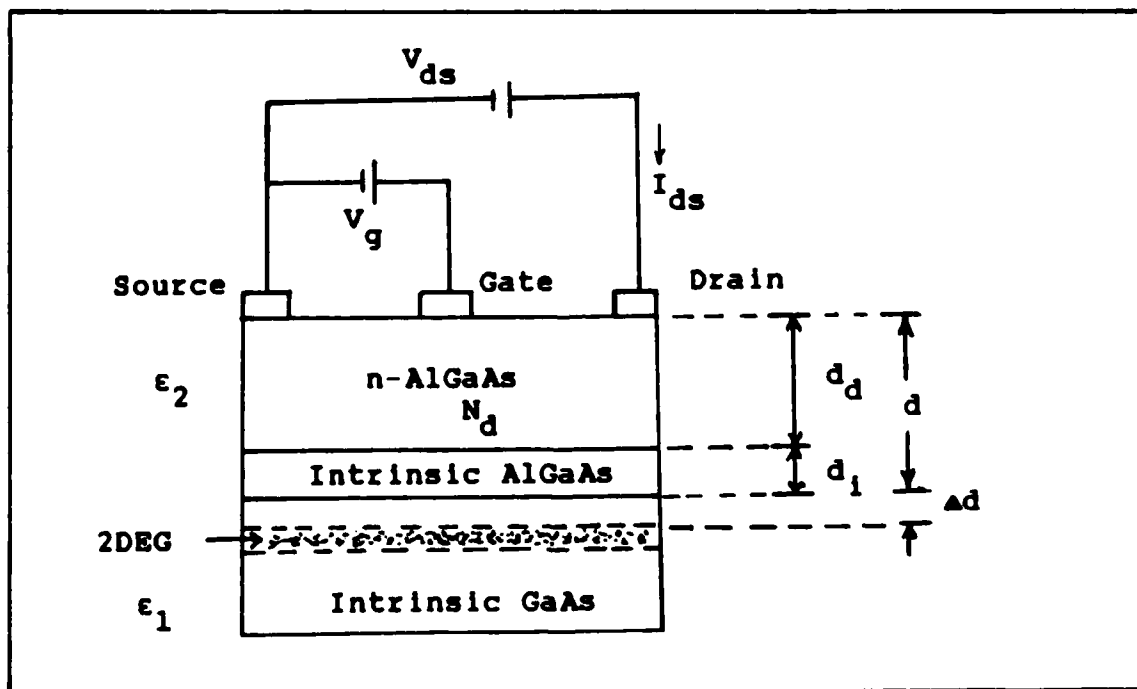


Fig 8. MODFET Dimensions.



Rewriting Eq 1,

$$n_s = \frac{\epsilon_2 [V_g - (\phi_b - \Delta E_c - V_{p2})]}{q(d + \Delta d)} \quad (4)$$

In the depletion mode (normally on), the surface depletion region just extends to the GaAs-AlGaAs interface depletion region. Application of negative gate bias will turn the device off by depleting the electron gas. This structure is generally used for discrete applications, such as microwave low-noise amplifiers, since the power consumption is too high for large scale integration (2:32).

In enhancement mode (normally off) devices, the gate is recessed further than in depletion devices; that is,  $d_d$  is small. This type of device, with low power dissipation, is used as a switch in high-speed digital integrated circuits (2:32). The gate built-in voltage depletes the doped AlGaAs, overcomes the built-in potential at the heterointerface, and depletes the electron gas. No charge flows from source to drain unless a positive gate voltage, greater than the threshold voltage,  $V_{off}$ , is applied. However, there is a maximum value of voltage associated with this before the parasitic MESFET in n-AlGaAs begins to conduct. Also, leakage in the Schottky diode occurs above that maximum. That maximum gate voltage is 0.6 to 0.8 V (3:1-1).

I-V Characteristics. When a drain to source voltage,  $V_{ds}$ , is applied, current,  $I_{ds}$ , flows in the source-drain

path. It is regulated by the voltage applied to the Schottky barrier gate (20:209):

$$I_{ds} = \frac{\epsilon_2 W}{d + \Delta d} [(V_g - V_{off})V_{ds} - 0.5V_{ds}^2] \quad (\text{mA}) \quad (5)$$

where  $W$  = gate width ( $\mu\text{m}$ ).

Equation 5 applies for  $V_{gs} < V_{gs,sat}$ , the source to gate saturation voltage. Equation 5 and experimental data for a typical MODFET are plotted in Fig 9.

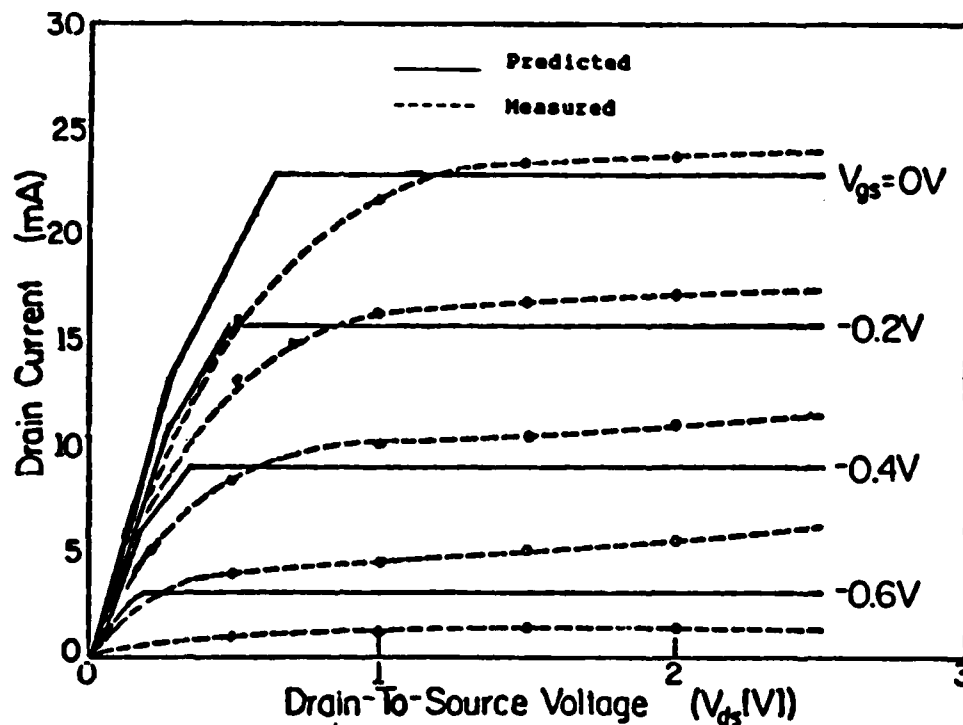


Fig 9. Output Characteristic for MODFET (20:211).

The speed of operation of a FET is determined in part by its transconductance. The larger the transconductance (slope of drain current versus gate voltage), the higher the

device speed. An approximate equation for transconductance is given for short gate lengths (3:2-27):

$$g_{m0} \approx \frac{\epsilon_2 W v_s}{(d + \Delta d)} \quad (6)$$

$g_{m0}$  = intrinsic transconductance (mS)

$v_s$  = saturated drift velocity of electrons in the 2DEG.  
(cm/s)

$W$  = gate width

In the MODFET, the denominator of (6) is nearly independent of bias, and  $g_{m0}$  remains nearly constant until the device is biased near pinchoff.

The extrinsic transconductance,  $g_m$ , that is observed at the external contacts, is lower than  $g_{m0}$  owing to parasitic source resistance. This quantity is related to the extrinsic transconductance by

$$g_m = \frac{g_{m0}}{1 + g_{m0} R_s} \quad (\text{mS}) \quad (7)$$

where  $R_s$  is the source resistance of the MODFET ( $\Omega$ ).

The transconductance of a device may also be defined as a change of drain current with respect to a change in gate voltage, for a given drain voltage (22:176). It is an indication of the amplification (gain) capability of the device. As Fig 10 shows, the MODFET at 77 and 300 K exhibits a steep  $I_{ds}$  versus  $V_g$  curve. Compared to a metal-oxide semiconductor (MOSFET) and MESFET, the MODFET has a high  $g_m$ .

This is also a direct result of the higher electron saturation velocity,  $v_s$ , in the MODFET. The higher transconductance means that the MODFET amplifies gate voltage very well, leading to a high gain.

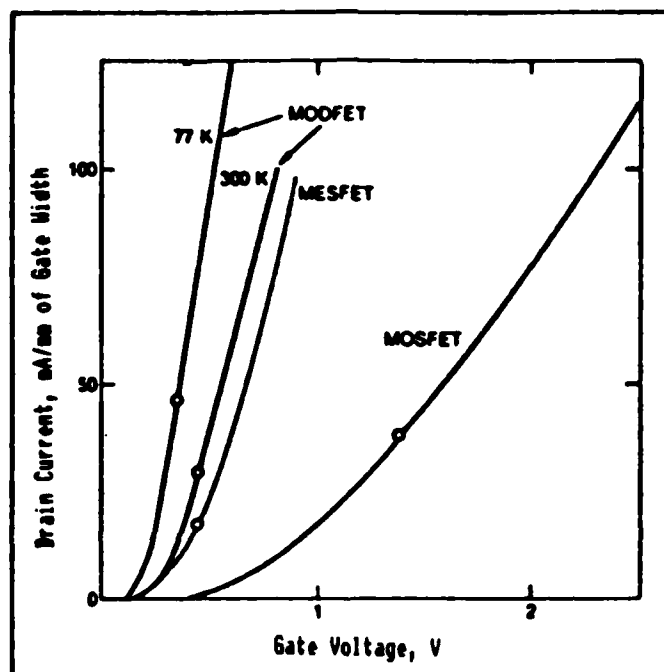


Fig 10. Drain Current Versus Gate Voltage Characteristic of the MODFET, MESFET, and MOSFET Devices (2:32).

As stated earlier, the parasitic MESFET in the AlGaAs layer and gate leakage current limit the maximum gate biasing voltage of normally-on MODFETs. That limit is approximately 0.8 V. Ostensibly, the problem could be overcome by choosing a gate metal that produces a higher Schottky barrier height,  $\phi_b$ . Unfortunately, the range of available metals with sufficient work functions and acceptable physical contact to an AlGaAs layer is severely limited. In

addition, the presence of interface states and a thin interfacial layer also reduce the range of available Schottky barrier heights (7:537).

#### Enhanced Schottky (ES) MODFETs

The development of ES MODFETs was undertaken in response to the limited gate voltage which can be impressed on a MODFET. In principle, if the Schottky barrier height can be increased, higher gate voltages can be realized. This, in turn, leads to lower gate leakage, higher signal-to-noise ratio, and less conduction through the AlGaAs parasitic MESFET at moderate gate voltages. This improvement leads to a wider range of amplifier applications for the device.

Shannon (7) has suggested that device designers need not be limited to Schottky barrier heights that can be realized from the limited number of materials and semiconductors. Instead, doped surface layers between the gate metal and semiconductor may be used to provide the desired barrier height. The surface layer must have a net space charge opposite in sign to that of the depleted part of the bulk semiconductor.

Highly doped n-type surface layers decrease the Schottky barrier height, and  $p^+$ -layers increase the height. Since the ES MODFET design increases the barrier height, only the  $p^+$ -layer will be discussed further.

Figure 11 shows the conduction band diagram for a Schottky diode. Figure 12 shows a conduction band diagram for a metal- $p^+$ -n structure where the materials have differ-

ent bandgaps. Clearly, the energy band in the semiconductor is distorted by the  $p^+$ -layer. The surface potential of the n-type layers at the gate is raised by the  $p^+$ -layer, if the  $p^+$ -GaAs doping is much higher than the n-AlGaAs doping (9:434).

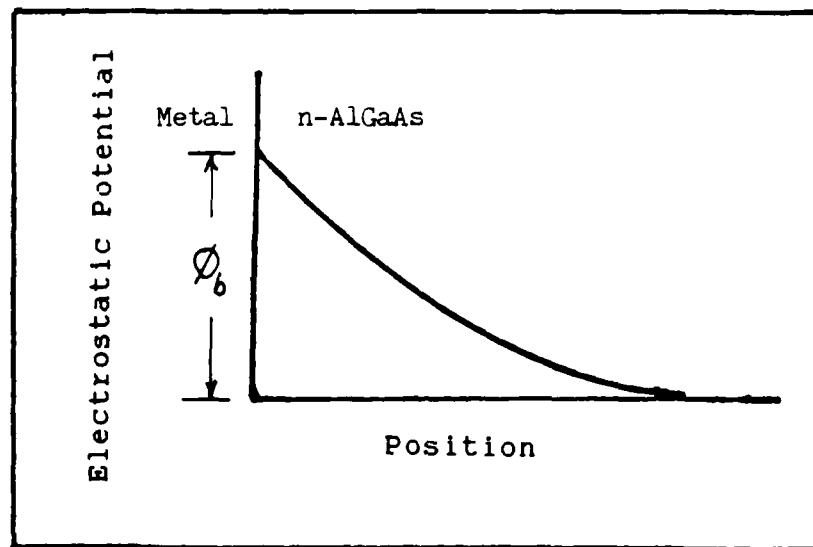


Fig 11. Conduction Band Diagram for Metal-Semiconductor Junction.

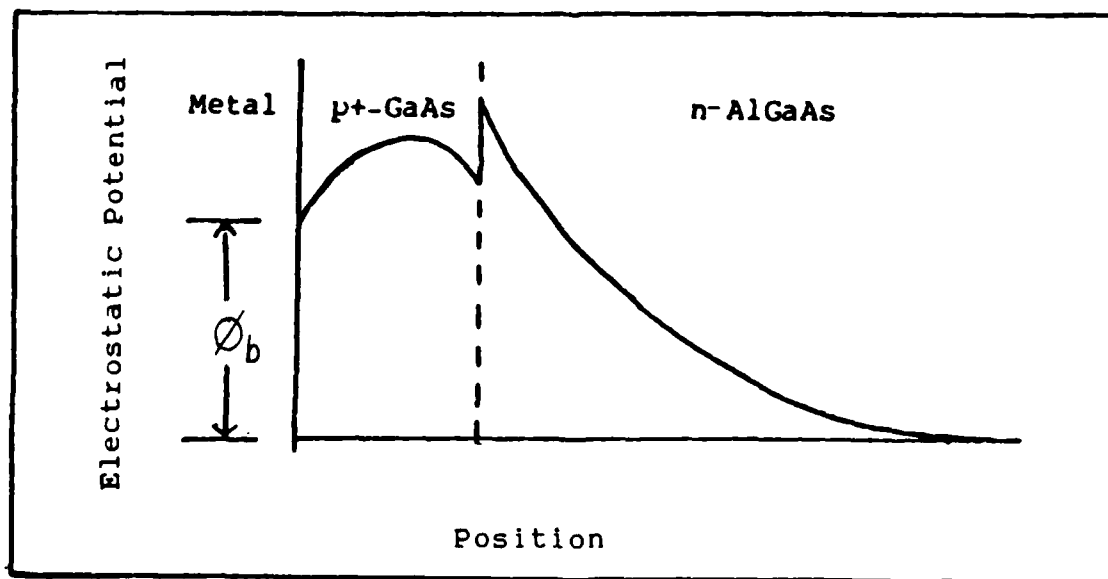


Fig 12. Conduction Band Diagram for Metal- $p^+$ -n System with Different Bandgaps (3:2-17).

Structure and Fabrication. The structure of the ES MODFET is identical to that for the standard MODFET (Fig 3), with two exceptions. With the ES MODFET device, there is a  $p^+$ -layer beneath the gate, and the gate is not recessed (Fig 13). Fabrication of the two structures is also similar. With respect to standard MODFETs, undoped GaAs, intrinsic AlGaAs and n-AlGaAs layers are grown on a semi-insulating substrate. A GaAs  $p^+$ -layer is grown next. It is typically 75-100 Å thick and Be doped with the acceptor concentration ( $N_a$ ) approximately equal to  $10^{19} \text{ cm}^{-3}$ . An isolation mesa etch follows the growth. Source and drain contacts are evaporated onto and alloyed into the  $p^+$ -layer to form ohmic contacts. The gate is then patterned and the metal evaporated. Finally, the unique step of etching the  $p^+$ -layer outside the gate area is performed. This step ensures that no MESFET path exists in the  $p^+$ -layer.

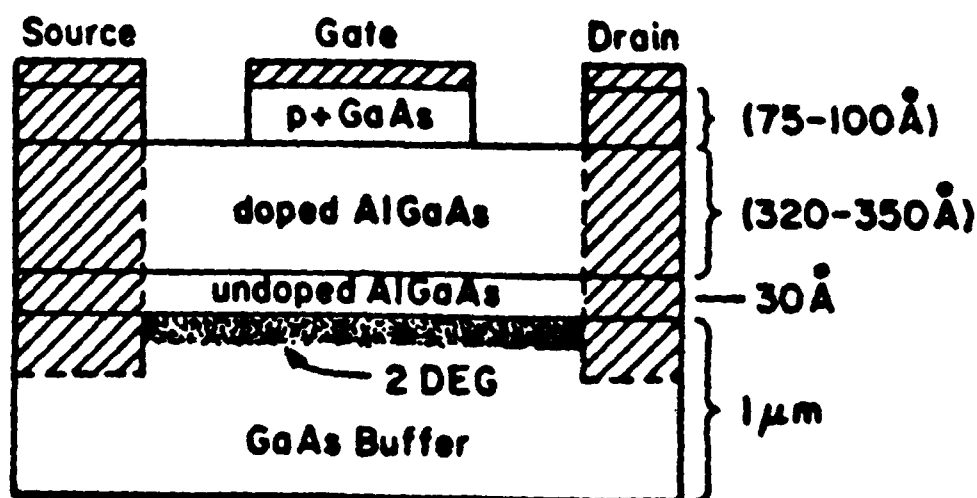


Fig 13. Cross-Sectional View of an ES MODFET (23).

Modes of Operation. Priddy (3) has charge control-modeled the electrostatic potential and electric field in the gate region of the ES MODFET, based on a solution of Poisson's equation, with known boundary conditions. It is known that, at each layer interface (Fig 14), the product of the dielectric constant and electric field,  $\epsilon E$ , is constant. Additionally, the electrostatic potential is constant across the boundaries, except for known discontinuities at heterointerfaces. A value for the Schottky barrier at the metal- $p^+$ -GaAs interface is assumed. Choosing a zero value of electrostatic potential at the 2DEG, potentials can be determined in the undoped AlGaAs, the n-AlGaAs and the  $p^+$ -GaAs.

It was shown that by varying the doping and thickness of the  $p^+$ -layer, the Schottky barrier height can be controlled. The higher the doping, the larger the barrier height. Also, the thickness of the  $p^+$ -layer must be chosen, in conjunction with the n-AlGaAs thickness, to deplete the n-AlGaAs layer for proper transistor operation, both in the depletion and enhancement mode. From a practical viewpoint, this must be considered because the gate of the ES MODFET can not be recessed without etching the  $p^+$ -layer. Recessing is the normal method for enhancing the electric field under the gate. Charge control for the ES MODFET is very similar to the standard MODFET in both enhancement and depletion modes, but the applied gate voltages necessary to effect a similar



change in conduction is higher. Equation 1 must be modified for the ES MODFET. Since the  $p^+$ -layer (Fig 14) has a thickness,  $t$ , the equations for distance between the gate and heterojunction must be modified relative to that of the standard MODFET (3:B-11). Therefore (3:B-11),

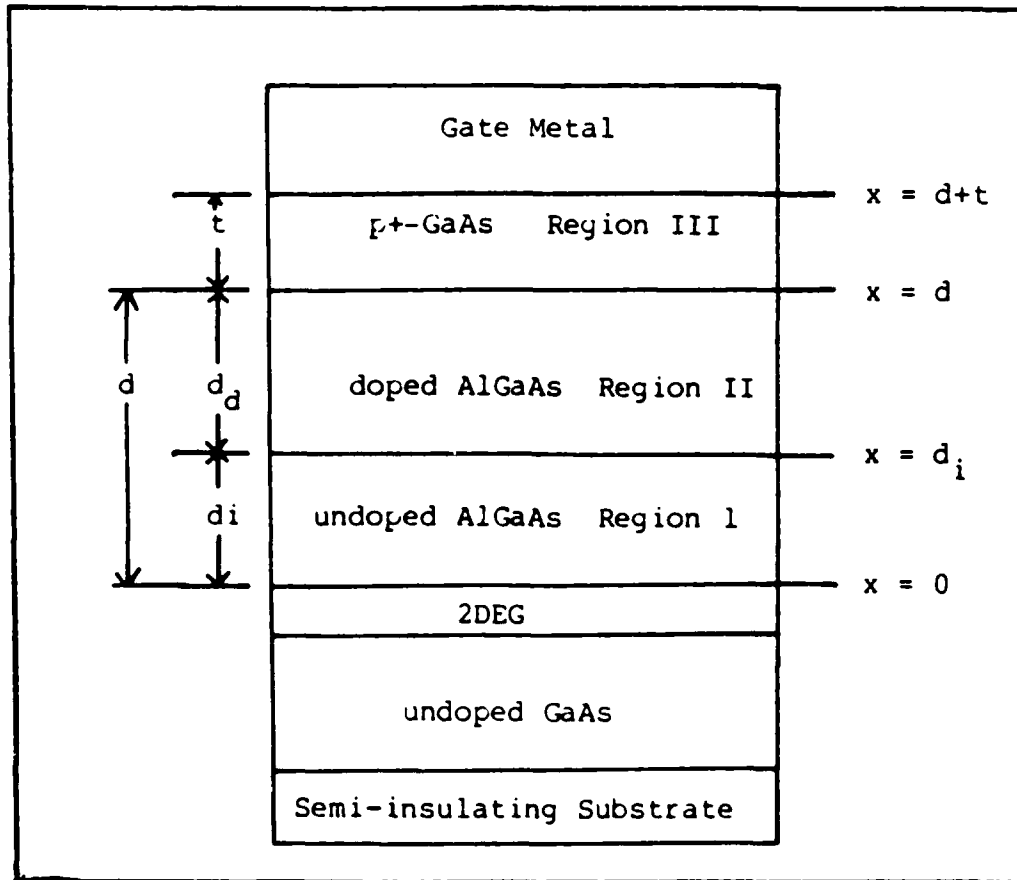


Fig 14. ES MODFET Structure Under the Gate Contact (3:B-2).

$$d' = d_d + d_i + \epsilon_2 t / \epsilon_1 \quad (8)$$

where,

$d'$  = effective distance between gate and heterojunction in ES MODFET (Å)

$\epsilon_1$  = dielectric constant of GaAs ( $F/cm^2$ )

$t$  = thickness of  $p^+$ -layer (Å).

In addition, the threshold voltage  $V_{\text{off}}$  is raised by the addition of the  $p^+$ -layer. The result can be expressed as:

$$V_{\text{off}}' = \phi_b + \frac{qN_a t^2}{2\epsilon_2} - \frac{qN_d d_d t}{\epsilon_1} - V_{p2} \quad (V) \quad (9)$$

where  $N_a = p^+$ -doping in GaAs cap layer ( $\text{cm}^{-3}$ ).

This leads to a new description of the ES MODFET 2DEG concentration,  $n_s'$ , which is:

$$n_s' = \frac{\epsilon_2}{q(d' + \Delta d)} (V_g - V_{\text{off}}') \quad (\text{cm}^{-2}) \quad (10)$$

The maximum barrier height,  $V_{\text{max}}$ , for the device is given by (3:4-3):

$$V_{\text{max}} = V_{\text{off}}' + \Delta E_c + \frac{qN_d d_d^2}{2\epsilon_2} \quad (V) \quad (11)$$

Substituting  $V_{\text{off}}'$  from Eq 9,

$$V_{\text{max}} = \phi_b + \frac{qN_a t^2}{2\epsilon_2} - \frac{qN_d d_d t}{\epsilon_1} + \Delta E_c. \quad (12)$$

The new barrier height is primarily dependent on the doping and the thicknesses of the n-AlGaAs and  $p^+$ -GaAs layers. It is also dependent on the discontinuity in the conduction band at the heterointerface of those layers.

An example calculation may be performed. Using correct constant values (22:513) and  $N_d = 3 \times 10^{18} / \text{cm}^3$ ,  $N_a = 2 \times 10^{19} / \text{cm}^3$ ,  $t = 100 \text{ \AA}$  and  $d_d = 320 \text{ \AA}$ , a value of  $V_{\text{max}}$  may

be determined. With  $\Delta E_c = 0.24$  V for the Al mole fraction  $x = 0.3$  (3:xi), the value of  $V_{max}$  is higher than  $\phi_b$  by 0.4 V.

A formula for the ES MODFET intrinsic transconductance ( $g_{m0}'$ ) based on the new effective gate-2DEG distance, is given as (3:2-27):

$$g_{m0}' \approx \frac{\epsilon_2 W v_s}{d' + \Delta d} \quad (\text{mS/mm}) \quad (13)$$

Since  $d'$  is greater than  $d$  for the standard MODFET, the device transconductance should decrease. For a comparison, see Eq (6).

I-V Characteristics. Fig 15 shows a gate I-V curve for an ES MODFET. Note that no significant gate leakage current flows until the gate voltage is above 1.3 V.

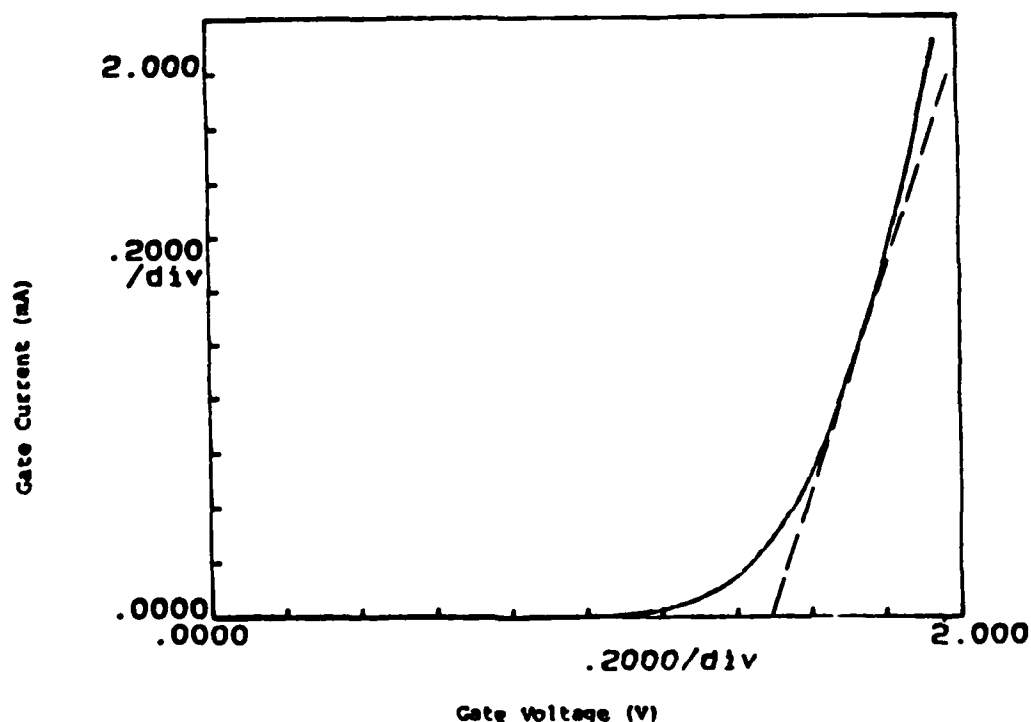


Fig 15. Gate I versus V Curve for ES MODFET Sample (3:D-18).

### Comparison of Standard and ES MODFETs

The barrier height for the ES device is significantly higher than for the standard MODFET, as the experimental data in Fig 16 indicates. This leads to a better noise immunity for the ES structure. A 3 dB increase in signal-to-noise ratio has been calculated (3:6-7). It is difficult for energetic carriers to overcome the Schottky barrier and cause noisy operation. The higher barrier also leads to increased reliability, since there is a smaller probability that a transient voltage spike at the gate will damage the device. Additionally, the presence of the  $p^+$  layer should reduce variability in device threshold voltages, which are due to poor layer thickness control. In addition,  $V_{off}'$  for the ES MODFET should be less sensitive to small fluctuations in the surface layer thickness when compared to  $V_{off}$  for a standard MODFET (10:604).

The ES MODFET has the added benefit of tailored barrier height. By control of  $p^+$ -layer thickness and doping, any barrier up to the AlGaAs barrier height can be selected (3:1-3). Therefore, the ES MODFET is more versatile.

### Pseudomorphic MODFETs

Another variation on MODFET structure is one in which an InGaAs/AlGaAs heterojunction system replaces the one consisting of GaAs/AlGaAs. Also called the strained quantum well MODFET, this device has certain advantages over the more widely studied GaAs/AlGaAs system.

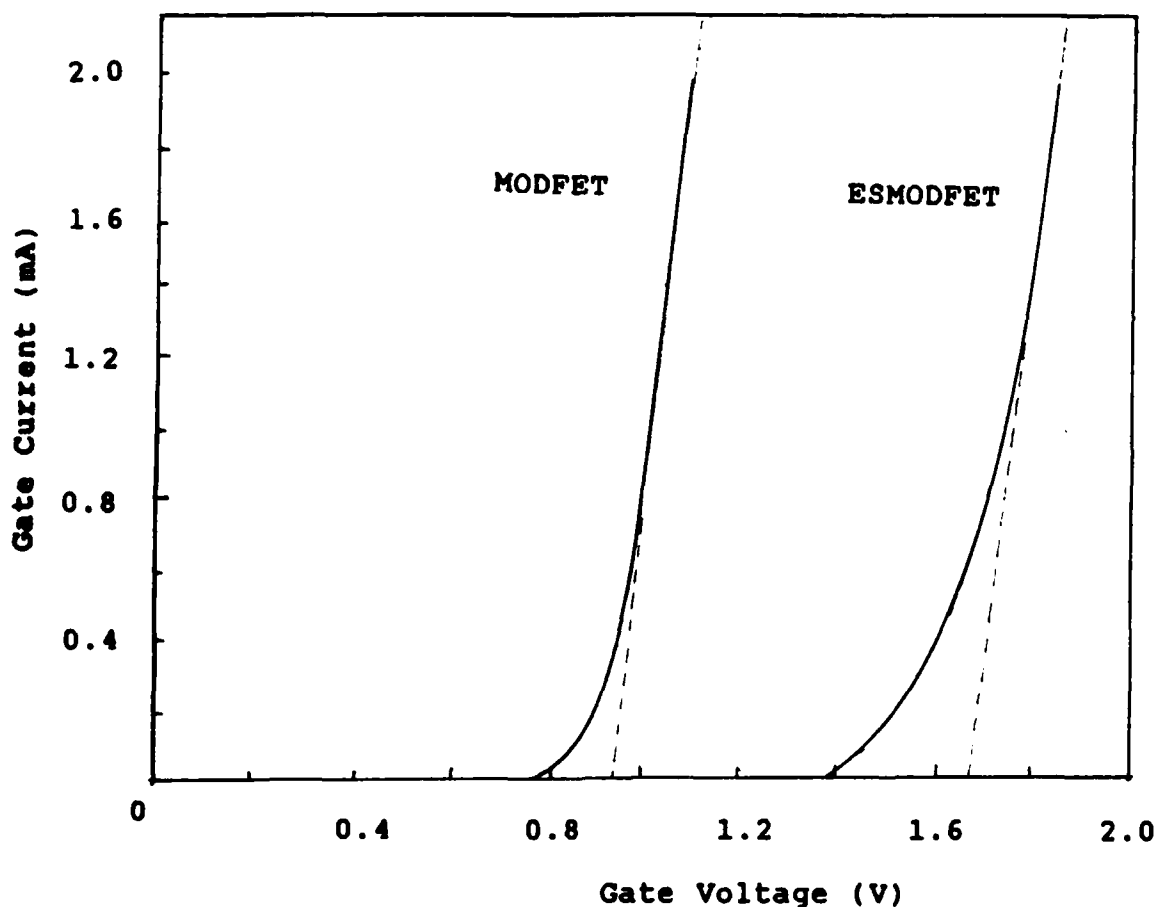


Fig 16. Gate I versus V Curve of MODFET and ES MODFET (3:6-7).

Need for Pseudomorphic MODFETs. In this structure, large conduction band discontinuities at the heterointerface,  $\Delta E_c$ , can be realized with a low mole fraction in the  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ . In the GaAs/AlGaAs system, an aluminum mole fraction greater than 0.2 is required to provide a sufficiently large  $\Delta E_c$ , which is necessary to minimize the

effects of hot electron injection and parasitic MESFET conduction (6:564). However, this high mole fraction is responsible for the problem of persistent photoconductivity. When exposed to light, MODFETs at low temperatures produce a photocurrent that decays over several days (2:35). Deep level traps (D-X centers) in the  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  are believed to be the cause (6:564). The InGaAs/AlGaAs pseudomorphic system avoids these problems with a lower Al mole fraction. This reduces the D-X occupation probability, but maintains the high  $\Delta E_c$ .

Also, electron saturated drift velocities,  $v_s$ , in the pseudomorphic MODFET are 20% higher than similar structures using GaAs (24:564). In low Al mole fraction  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ , there is also a lower trap density. Higher doping densities are also possible because of reduced donor concentration. The transconductance in the InGaAs MODFET may be superior because of a smaller average distance of the 2DEG from the heterointerface. This is due to improved carrier confinement in the quantum well (6:565), and to the higher saturation velocity in the InGaAs.

Structure and Fabrication. The structure of an InGaAs/AlGaAs MODFET is shown in Fig 17. It is essentially the same as a standard MODFET, but a layer of undoped  $\text{In}_y\text{Ga}_{1-y}\text{As}$  is interposed between the unintentionally doped GaAs buffer layer and AlGaAs. The 2DEG is confined in this layer. The y-mole fraction has varied from 0.05 to 0.2 in experiments to date (6:565). The InGaAs layer is lattice

mismatched to AlGaAs, but is sufficiently thin and the mismatch is accommodated entirely by elastic strain. A GaAs/-AlAs superlattice beneath the buffer relieves that strain. The interface between materials is essentially free from dislocations. The thin layer is therefore called "pseudomorphic" (25:491). The resultant band diagram is shown in Fig 18.

Pseudomorphic MODFETs have improved transport properties over standard MODFETs, because of greater carrier confinement and saturation velocity. However, they suffer the same limitations in barrier height as the standard MODFET. The next logical developmental step is to apply the technology used in ES MODFETs to pseudomorphic MODFETs. That is, the addition of the  $p^+$ -layer should increase the barrier height as it did for standard MODFETs.

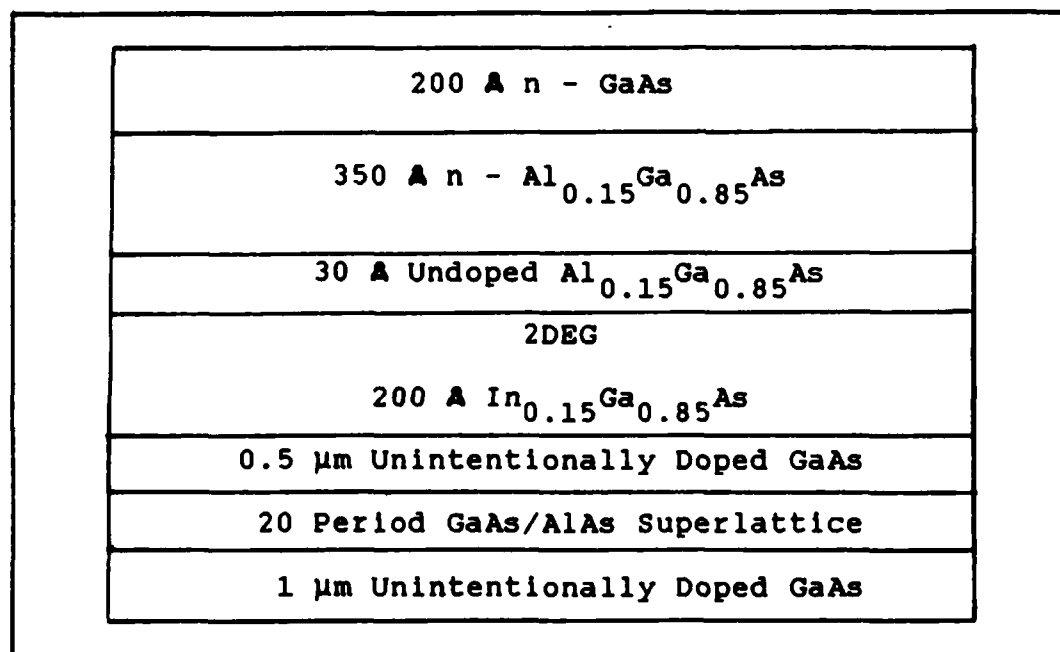


Fig 17. Typical Structure for MBE-Grown InGaAs/AlGaAs Pseudomorphic MODFET (24:629).

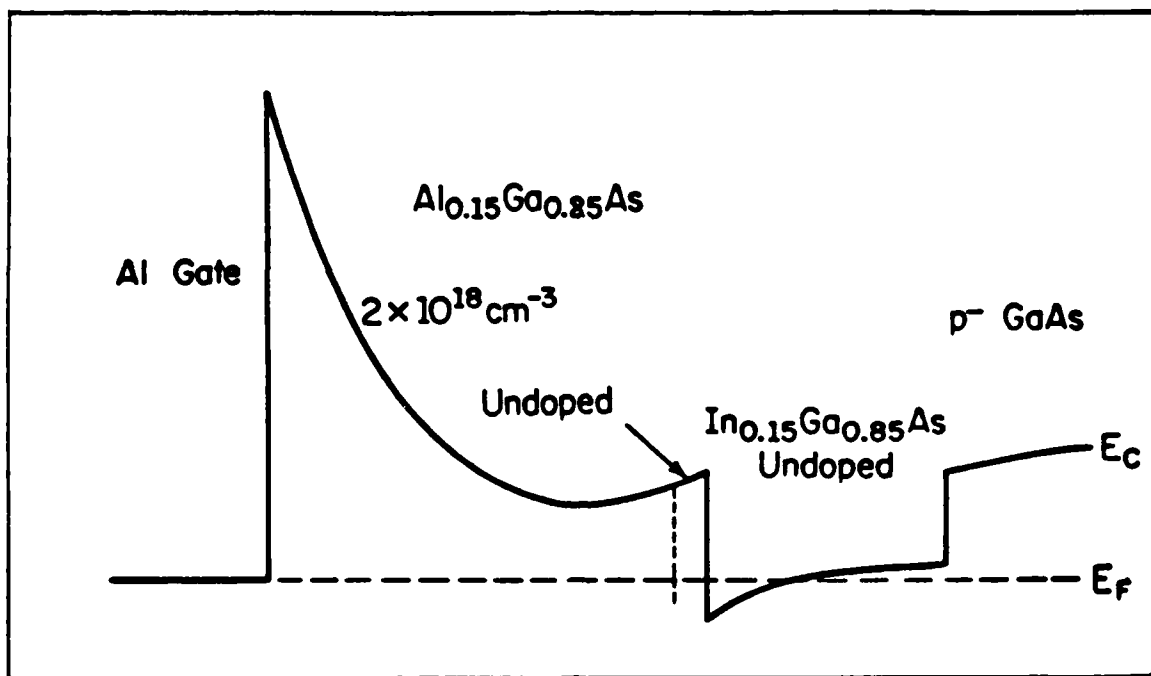


Fig 18. Conduction Band Diagram for InGaAs/AlGaAs MODFET. The Conducting Channel Forms a Two-Dimensional Electron Gas in the InGaAs Quantum Well (24:629).

#### Enhanced Schottky Pseudomorphic MODFETs

To realize the goal of enhanced Schottky barriers on pseudomorphic MODFETs, the structure of Fig 19 may be used. The layers are very similar to that for the pseudomorphic MODFET (Fig 17) including the GaAs/AlAs superlattice, but a  $p^+$ -layer is grown in place of the  $n^+$ -cap layer. FET structures are defined above this layer. The conduction band diagram may be modelled as for an ES MODFET, using the proper value of  $\Delta E_c$  for the pseudomorphic MODFET in the model derived in (3).

The primary purpose of this experimental effort is to evaluate the addition of the  $p^+$ -layer to the pseudomorphic MODFET and its impact on microwave and noise performance.



Parameters that will be used to characterize this impact must be defined and described.

100 Å p <sup>+</sup> - GaAs
350 Å n - Al <sub>0.15</sub> Ga <sub>0.85</sub> As
30 Å Undoped Al <sub>0.15</sub> Ga <sub>0.85</sub> As
2DEG
200 Å In <sub>0.15</sub> Ga <sub>0.85</sub> As
0.5 μm Unintentionally Doped GaAs
20 Period GaAs/AlAs Superlattice
1 μm Unintentionally Doped GaAs

Fig 19. Structure for MBE Grown ES Pseudomorphic MODFET.

#### Microwave Performance

Transistors used at microwave frequencies frequently operate as amplifiers. The device's ability to amplify signals with little noise at the highest possible frequency best characterizes their performance. Therefore, the most important considerations for a microwave transistor, in addition to its DC characteristics, are bandwidth, gain and noise (26:91).

To characterize the microwave response, standard figures of merit commonly used in microwave measurements will be studied for their ease of measurement and relevance to the bandwidth, gain and noise factors.

Unity Current Gain Frequency. This widely used figure of merit is defined in terms of the average time necessary for a charge carrier travelling at an average velocity ( $v_{avg}$ ) to traverse the channel of a field effect transistor (from source to drain or vice versa).

$$f_T = \frac{1}{2\pi t_d} \quad (\text{GHz}). \quad (14)$$

Here  $f_T$  is the unity current gain cutoff frequency, and  $t_d$  is the average time necessary for an electron to travel through the channel. This measure describes the frequency at which the device can no longer provide current amplification, and is therefore a measure of the bandwidth of the transistor. The delay ( $t_d$ ) is merely the gate length ( $L_g$ ) divided by the saturation velocity ( $v_{avg}$ ). Therefore,

$$f_T = \frac{v_{avg}}{2\pi L_g}. \quad (15)$$

In a wideband lumped circuit,  $f_T$  is expressed as (27:118):

$$f_T = \frac{g_{m0}}{2\pi C_{gs}} \quad (16)$$

where  $C_{gs}$  is the gate-to-source capacitance, and  $g_{m0}$  is the

intrinsic transconductance of the device. Under the short channel approximation (10:601),  $g_{m0}$  is given for a MODFET as

$$g_{m0} = \frac{C_{gs} v_s}{L_g} \quad (\text{mS}) \quad (17)$$

and

$$C_{gs} = \frac{\epsilon_s L_g W}{t_i} \quad (\text{pF}) \quad (18)$$

where  $v_s$  is the saturation velocity of carriers in the channel (cm/s),  $W$  is the gate width ( $\mu\text{m}$ ),  $\epsilon_s$  is the permittivity of the semiconductor material between the gate and the 2DEG ( $\text{F/cm}^2$ ), and  $t_i$  is the total thickness of that material ( $\text{\AA}$ ). Substituting Eq 17 into Eq 16 results in Eq 15, which shows that the cutoff frequency is only dependent on the saturation velocity of carriers in the 2DEG and the length of the channel.

Noise Figure. It is desirable for a transistor to amplify microwave signals without adding significant amounts of noise to the amplified signal. Noise is a function of frequency. Intrinsic noise sources in a FET include thermally-generated channel noise and noise induced at the gate. The gate and drain resistances of the FET, as well as bonding pad resistances, also increase the noise generated (26:36).

To provide a relative measure of how well a device amplifies without adding noise, another figure of merit was developed. The overall effect of many noise sources in a

microwave transistor is frequently specified via the noise figure (NF) of the circuit. The noise figure of any two-port network can be defined in terms of its performance with a standard noise source connected to its input terminals (27:122).

$$NF = \frac{\text{Available noise power at output}}{\text{Available noise power at input}} = \frac{P_{no}}{GkTB} \quad (19)$$

where  $GkTB$  is the available noise power of a standard noise source in a bandwidth  $B$  at temperature  $T$  with Boltzmann's constant  $k = 1.381 \times 10^{-23}$  J/°K. This product is the input noise power,  $P_{ni}$ , where  $G$  is the available power gain of the network at the bandwidth considered, and  $P_{no}$  is the available noise power at outputs. That quantity,  $P_{no}$ , arises from noise generated within the network and from the amplification of the input noise.

Noise figure may also be defined as the ratio of the available signal-to-noise power ratio at the input,  $P_{si}/P_{ni}$  to the available signal-to-noise power ratio at the output,  $P_{so}/P_{no}$  (26:140):

$$NF = \frac{P_{si}/P_{ni}}{P_{so}/P_{no}} \quad (20)$$

This follows directly from Eq 18, where  $G$  is defined as the ratio of output signal power to input signal power.

Obviously, it is desirable to minimize NF. At microwave frequencies, the input and output powers are a function of

the impedance match of the input and output circuitry to the amplifying transistor. A perfect input and output conjugate impedance match minimizes NF.

Noise performance is dependent on gate bias and, to a lesser extent, on drain bias (28:245). A typical drain bias dependence of NF for a GaAs FET is illustrated in Fig 20. Drain bias is normalized to its saturated value at zero gate bias,  $I_{dss}$ , for a depletion mode device.

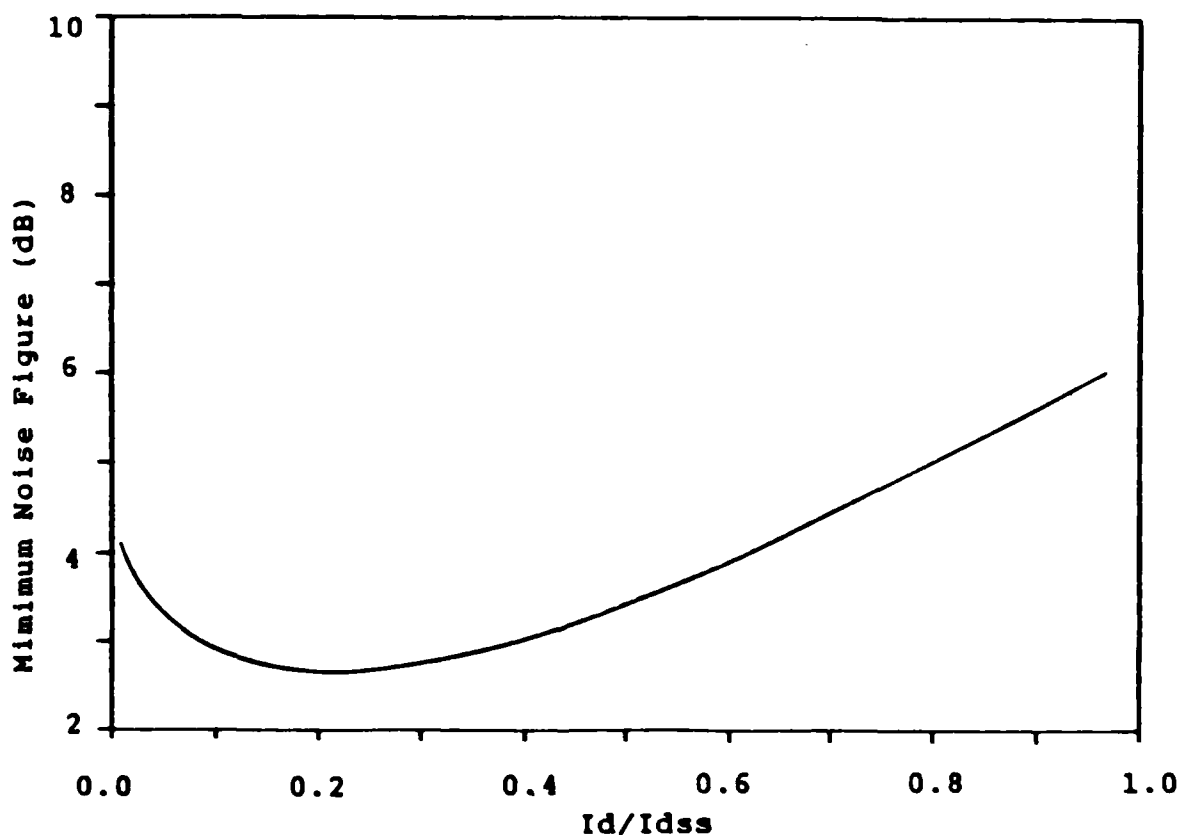


Fig 20. Noise Figure versus Normalized Drain Current for a Typical Depletion-Mode GaAs FET at 10 MHz (28:246).

In summary, NF is a figure of merit that depends on frequency, device noise generation, impedance matching and bias conditions. It is, nevertheless, a useful descriptor

of FET amplifying performance when properly applied.

Maximum Frequency of Oscillation. The power gain of a transistor is another important descriptor of its microwave performance. The frequency where the maximum available power gain of the transistor ( $G_{A,max}$ ) falls to unity is called the maximum frequency of oscillation ( $f_{max}$ ) (26:32).  $G_{A,max}$  falls off with frequency at a rate of 6 dB/octave in microwave transistors (26:33).

#### Summary.

Four different variations on the MODFET structure have now been outlined. The structural characteristics of these devices are summarized in Table I. Their relative performance can be measured at microwave frequencies. Bandwidth capability can be quantified through the measurement of  $f_T$ . Noise performance is based on the measurement of NF. The relative capability of the devices to amplify may be indicated via the measurement of  $f_{max}$ .

Table I. Summary of Different MODFET Structures.

Device	Structure	$p^+$ beneath gate
Standard MODFET	AlGaAs on GaAs	No
ES MODFET	AlGaAs on GaAs	Yes
Pseudomorphic MODFET	AlGaAs on InGaAs	No
ES Pseudo-morphic MODFET	AlGaAs on InGaAs	Yes

### III. Equipment

Equipment used in this effort included fabrication, packaging and test equipment. FETs were fabricated on MBE-grown films using standard microelectronic laboratory equipment in two different clean room facilities: that of the University of Illinois (UI) and one at the Air Force Wright Aeronautical Laboratory's Air Force Avionics Laboratory (AFAL). Additional equipment was then used to dice and package the finished devices at AFAL. Finally, DC and microwave test instrumentation was used to evaluate device performance after packaging.

#### Fabrication Equipment

Manufacturing MODFETs from MBE-grown material requires a photoresist spinner, curing ovens, a mask aligner and mask set, metal evaporation system and alloying oven.

Photoresist Spinner. A photoresist spinner was utilized to deposit thin, uniform layers of positive photoresist on wafers for subsequent processing. The photoresist spinner assembly consists of the spinning chuck and the unit which controls spin speed and duration. A vacuum pump attached to the photoresist spinner secures the wafers in place. A Headway Research model was used at UI and a Solitec unit at AFAL.

Curing Ovens. Small hot plate ovens at different temperatures were used for drying wafers, and for pre- and post-baking photoresist. Thermolyne OV-10600 ovens were

used at 70°, 90° and 110° C at UI. Precision Corporation mechanical convection ovens were used at 70, 90 and 150° C at AFAL.

Mask Aligner and Mask Set. A Karl Suss model MTB 3HP UV400 mask aligner was used at UI and a Karl Suss MJB-3 at AFAL. After mask alignment, wafers were exposed to ultra-violet light for a period long enough to fully solubilize the photoresist in use.

Evaporation System. Electron gun and thermal evaporation systems were used for the evaporation of the metal contacts and overlays onto the wafer surfaces at high vacuum. A Perkin-Elmer bell-type chamber was used at UI (Ultek RCS model) and a Temescal FC-1800 evaporation system was used at AFAL. Evaporation pressures were typically on the order of  $10^{-6}$  torr. Evaporated metal thicknesses were measured with a Sloan DTM crystal monitor at UI and an Inficon IC 6000 thickness monitor at AFAL.

Alloying Oven. The alloying equipment at UI consists of a small cylindrical oven, a Eurotherm temperature controller and a Matheson model 836 hydrogen purifier. After the source and drain contacts were evaporated in the chamber, they were alloyed at 500° C in the oven to form ohmic contacts. At AFAL, a Heatpulse 210 rapid transient alloying oven was used at 425° C.

#### Packaging Equipment

Finished MODFETs were diced and mounted in headers to facilitate noise figure testing. A Micro Automation model



1006 wafer saw was used at AFAL. Single MODFETs were diced from the wafer and bonded to microwave stripline carriers (Fig 21). Next, the bonding epoxy was cured in a Blue M OV-475A-2 oven. Wire bonds were made with a Kulicke & Soffa 4123 wedge bonder.

### Test Equipment

DC testing was performed at several points throughout the fabrication process. This ensured control of device quality and identified steps in the fabrication procedure which were critical. At the completion of the fabrication process, both DC and microwave measurements were performed.

DC Test Equipment. At the successful completion of the fabrication process, a DC test apparatus was used to determine device characteristics. Relatively simple tests were performed on the devices before dicing, to select devices for packaging and microwave testing. Devices were placed on a probe station which was connected to a Hewlett-Packard (HP) model 4145 semiconductor parameter analyzer. I-V characteristics and transconductance measurements were taken with this instrument. An HP 7475 plotter was connected to the analyzer via a Hewlett-Packard Interface Bus (HP-IB) to obtain hard copy I-V and transconductance plots.

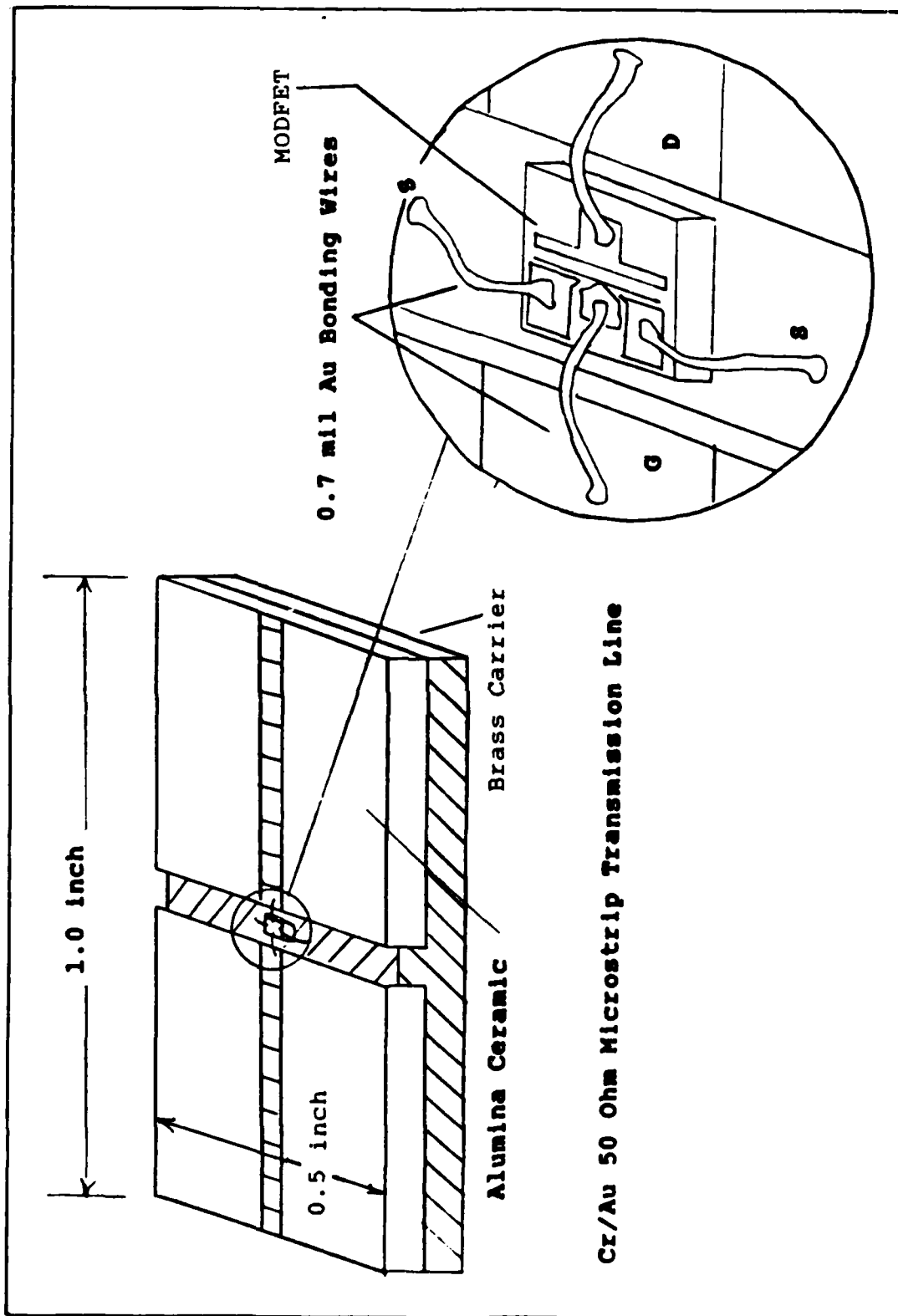


Fig 21. Chip Carrier and Bonding Scheme (inset) (29:7).

One unique advantage of the HP 4145 analyzer is its current and voltage limiting capability. This greatly reduced the destruction of voltage-sensitive MODFETs caused by voltage overstress. Also, measurement settings could be stored in the analyzer and retrieved periodically. Use of this capability reduced measurement error due to incorrect use of parameters and significantly reduced measurement time.

Microwave Measurements. These measurements were the final step in the experimental process. S-parameter measurements were performed on the devices. Computed figures of merit ( $f_T$  and  $f_{max}$ ) were then obtained from this data. A rather complicated microwave network analysis system was used to obtain the S-parameters.

Network Analysis System. To measure S-parameters, the HP 8409C automated network analysis system, whose components are enumerated in Table II, was used as configured in Fig 22.

This automated network analyzer system provides control of the source output frequency, test set switching, receiver tuning, gain, measurement and conversion of data. This produces error corrected transmission and reflection measurements ranging from 2 to 18 GHz with a minimum of operator intervention. The system consists of a source, test set and receiver instrumentation, a source phase-lock subsystem, and a desktop computer with an HP-IB interface. The 9845B desktop computer controls the source, the relay actuator,

and the analog-to-digital converter, all via the data bus. The relay actuator in turn controls the S-parameter selection on the 8743B test set.

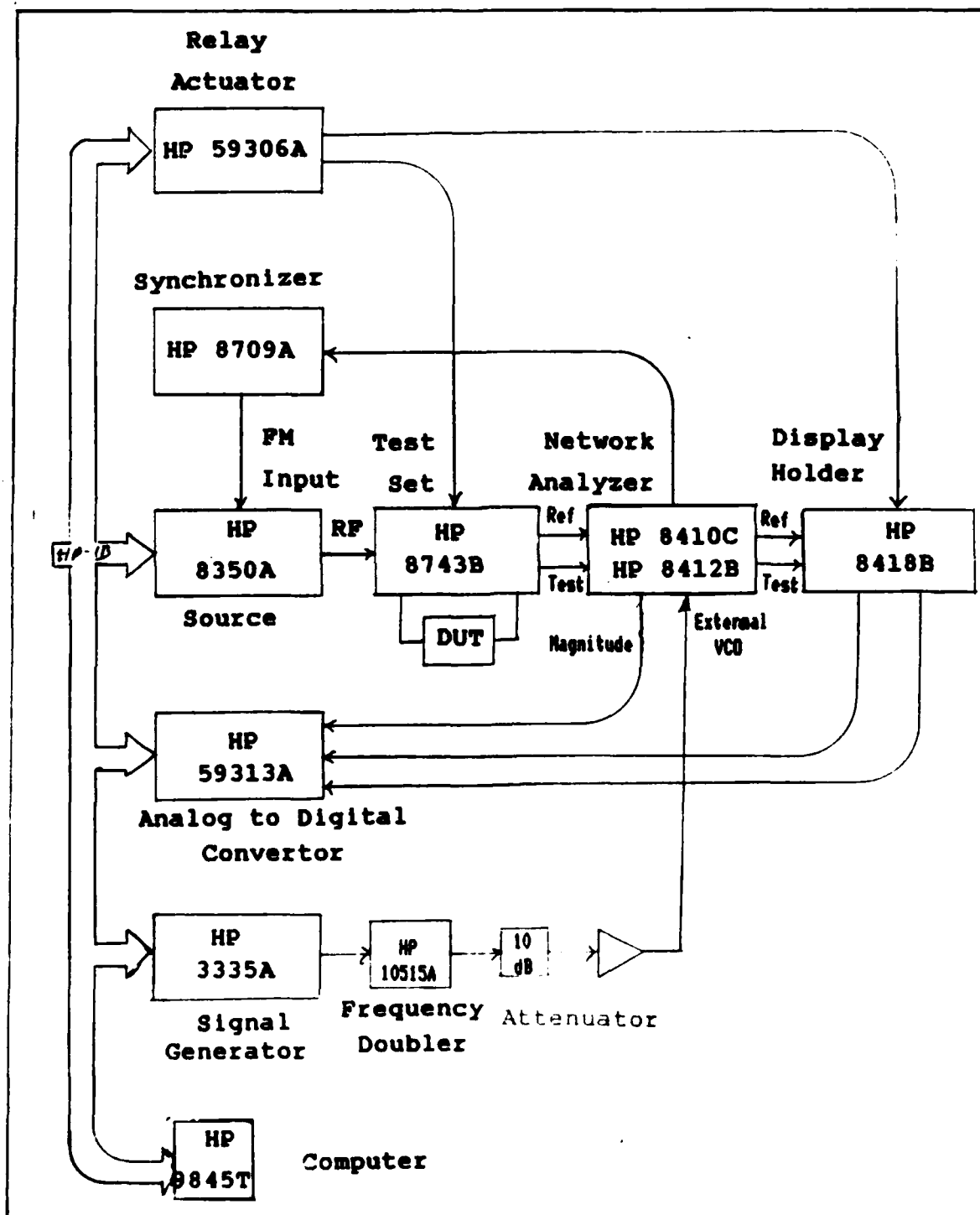


Fig 22. Configuration of Network Analysis System.

Table II. HP 8409C Automatic Network Analysis Equipment.

Manufacturer	Model Number	Nomenclature
HP	8410C	Network Analyzer
HP	8412B	Phase Magnitude Display
HP	8414B	Polar Display
HP	59306A	Relay Actuator
HP	59313A	HP-IB Analog-Digital Converter
HP	8350A	Sweep Oscillator
HP	86290B	RF Plug-in
HP	3335A	Synthesizer/Level Generator
HP	8709B	Synchronizer
HP	11859A	Amplifier Switch
HP	8447E	Amplifier, 0.1-1300 MHz
HP	8743B Opt 018	Reflection/Transmission Test Set
HP	6224B	Voltage Supply (2)
HP	3465B	Digital Multimeter
HP	11590A	Bias Network (2)
HP	9845B	Desktop Computer
Cascade	Prototype	Microprobe Station

For each measurement, the computer programs the 8350A sweep oscillator to a continuous wave (CW) frequency. The signal is directed to the 8743B reflection/transmission test

set. The 8743B provides splitters and couplers necessary to transmit a signal to the device under test (DUT). It also routes reference and response signals to the 8410C. Interposed between the 8743B and DUT is the 11590A bias network, which couples voltages to the DUT. The 11590A accepts as inputs, DC drain and gate bias voltages from the power supplies, and RF signals from the 8743B. It couples each of these to the DUT, while isolating DC and RF supplies from each other. The DUT is probed by the Cascade Microprobe station, which is attached to the 8743B by coaxial cable. The 8410C vector network analyzer performs actual response measurement. Reference and response data are input to the analyzer. Both signals are down-converted to intermediate frequencies (IF), where low frequency circuitry can measure amplitude and phase relationships (30:2-3). Analog displays and signals of device response are available on the 8412B and 8418B. Those signals are then digitized by the HP 59313A analog-to-digital converter.

A source phase-lock subsystem is incorporated into the network analysis system to provide synthesizer-class frequency accuracy and repeatability. By phase-locking the network analyzer to the source, small magnitude and phase errors are eliminated (31:1), resulting in a very stable and accurate stimulus signal for high frequency measurements. The phase-lock subsystem consists of the 3335A synthesizer and 8709B synchronizer.

Network analysis measurements are automated as pre-scribed in reference (31). The 59313A converts analog data to a Hewlett-Packard Interface Bus (HP-IB) compatible form. That data is sent to the 9845B computer. Using the HP BASIC software package 11863D, (Accuracy Enhancement Pac) the 9845B performs calibrations, manages data collection and converts raw S-parameter data into descriptive microwave parameters. It then tabulates, graphs and outputs data and computed parameters on an integral printer.

The 8409C measurement system must be calibrated before accurate measurements on devices can be made. During the measurement calibration sequence, the computer measures and stores vector (phase and magnitude) error terms. A precision fixed or sliding load, a short circuit, a shielded open circuit and a "through" connection are each connected at the measurement reference plane. Measurement of these terminations allows the computer to quantify directivity, source impedance match, load impedance match, isolation and tracking errors. This is done at each frequency where device measurements are later made. Those systematic errors are then removed from device response during the measurement sequence as the analyzer tunes back to each frequency where calibration was accomplished. The result is accurate, high resolution magnitude and phase data. Pertinent accuracy specifications of the network analysis system (ref 45) are tabulated in Table III.

Table III. Accuracy Specifications of Phase-Locked 8409C System (ref 32).

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Measurement Resolution	0.01 dB 0.1 nanosecond 0.1 degree 100 Hz frequency
Frequency Coverage	2-18 GHz (with 8743B Test Set)
Phase Lock	better than 1 Hz
Measurement Repeatability (phase lock mode)	.05 dB, 0.5 degrees (short term)

The manufacturer recommends periodic functional checks of the system, in addition to daily calibrations (31:23). This ensures that system hardware and software performance is within standards. An air line, attenuator or short circuit termination provides reasonable information on system performance, when their responses are compared to historical data. Even more detailed examination of performance characteristics can be made by periodically measuring one or more standard devices and comparing with historical data (31:23).



#### IV. Experimental Procedure and Results

This chapter describes the procedures undertaken to reach the intended goal of fabricating, testing and comparing the microwave performance of MODFET structures with and without  $p^+$ -layers under the gate.

Before fabrication of MODFETs, MBE growth parameters were chosen. The choices were based in part on theoretical calculations obtained from the charge control model. They were also based on past DC experimental performance of AlGaAs/GaAs ES MODFETs. Pseudomorphic MODFET growth parameters were then communicated to the University of Illinois Coordinated Sciences Laboratory. That laboratory used those prescribed parameters to grow pseudomorphic MODFET wafers by MBE.

After MBE growth, the general approach taken was to fabricate and test pseudomorphic and ES pseudomorphic MODFETs from the same MBE-grown material. This approach was implemented to minimize the growth and processing variables between similar samples. For example, MBE growth parameters may vary substantially from one growth run to another, despite attempts to control them. These variables may include actual growth rates, doping and flux calibrations, and sample purity. Fabricating different device types from a common substrate minimizes these variables. This approach does not preclude the possibility of a spatial dependence of device characteristics on one wafer, due to non-uniform

crystal growth.

Also, fabrication and test procedures for the control (no  $p^+$ -layer) devices and ES devices were performed as identically as possible, to minimize uncontrollable process variations. In fact, ES and control devices were fabricated at exactly the same time, under identical circumstances, on the same wafer. Only after source-drain metallization were the control and ES samples even discriminated, and the wafer chip scribed into control and ES samples. From this point on, the only fabrication difference was the etching of the  $p^+$ -layer on the control samples, prior to gate metal deposition.

Different fabrication procedures were, however, used for different parts of the same wafer. After MBE growth, wafer chips were scribed from the grown wafer. Some chips were then used to fabricate devices at the University of Illinois (UI), while others were sent to the Air Force Avionics Laboratory for the fabrication of ES and control devices. Significantly different fabrication procedures were used at the two laboratories, owing to differences in equipment and personnel. This parallel fabrication approach was used to take advantage of the extensive fabrication experience at UI, and to determine if MBE growth runs were suitable for further fabrication and extensive measurement.

In past efforts at fabricating ES MODFETs, there has been a persistent problem with etchants used to remove the  $p^+$ -layer on the control samples, and for etching that layer

between source, gate and drain contacts on the ES device. Some effort was made in this study to address these problems and to properly etch the devices.

After fabrication and etching, all samples were tested at DC to discern which samples were suitable for further microwave testing. It was at this point that several samples were rejected, owing to the absence of desired characteristics. These characteristics included successful fabrication of both ES and control samples by the same growth and fabrication process, source and drain contact ohmicity, and sufficient transconductance to produce a measurable gain on the network analyzer.

Next, acceptable devices were tested in the network analyzer. They were then diced and bonded into microwave stripline carriers. A final DC check was then performed to ensure that the device was packaged properly before noise measurement.

This chapter will describe in detail all of the above procedures including MBE parameter determination and growth, fabrication, etching, DC testing and microwave testing.

#### MBE Parameter Determination and Growth.

The selection of growth parameters for ES pseudomorphic MODFETs was based in large part on the experience of personnel at UI and AFAL and on published results. For previously reported pseudomorphic MODFETs,  $N_d$  was  $3 \times 10^{18}$  in a 350 Å AlGaAs layer. The Al mole fraction was  $x = 0.15$ , and the

indium mole fraction in the undoped InGaAs layer ( $y$ ) varied from 0.05 to 0.2 (6:565). Overall, best results were obtained with  $y = 0.15$ . With this value of  $y$ , saturation velocities were maximized. While higher transconductances were obtained with  $y = 0.20$ , lower values of  $y$  produced fewer deep level traps. The 0.15 value represents a trade-off of these two phenomena (6:570).

To choose parameters for the  $p^+$ -layer, the results from the previous work on ES MODFETs (3) were considered. Highest barrier shifts were obtained from samples which used 100 Å  $p^+$ -layers. Because the observed barrier heights in that effort varied widely, higher  $p^+$ -layer dopings were used in these experiments in an attempt to provide as high a barrier as possible.

For this effort, all pseudomorphic samples were grown with a 10-period superlattice of 50 Å GaAs and 20 Å AlAs. A 1 µm buffer layer was grown next, followed by a 150 Å layer of unintentionally doped InGaAs with  $y = 0.15$ , nominally. Next, 30 Å spacer layers were grown, followed by n-doped AlGaAs with  $x = 0.15$ , and the  $p^+$ -layer. Differences between pseudomorphic samples are outlined in Table IV. Sample numbers reflect University of Illinois MBE growth numbers.

The band structures of the devices were modelled using a computer program developed by Priddy (3) based on his study. The program utilized the charge control model to plot conduction band potentials, based on the solution of Poisson's

equation under the gate. The program solves the equation in each region of the device above the 2DEG (intrinsic AlGaAs, n-AlGaAs and  $p^+$ -GaAs regions), from knowledge of the boundary conditions at each interface. Layer dopings and thicknesses were also used as inputs. It was known that the product of the dielectric constant and electric field,  $\epsilon E$ , is constant across each interface. The electrostatic potential was not constant across each interface, but differed at heterointerfaces by the known conduction band discontinuity,  $\Delta E_c$ . The potential at the Schottky barrier,  $\phi_b$ , was assumed to be 0.8 V. With all boundary conditions, layer compositions, dopings and thicknesses as inputs, the electrostatic potential was calculated and plotted. The peak electrostatic potential was  $V_{\max}$ , whose value was also computed from Eq 12.

The modelling program is given in Appendix A. The results for samples 2812, 2815 and 2816, based on layer data in Table IV, are given in Figs 23, 24 and 25. In each case, the addition of the  $p^+$ -layer significantly raised the Schottky barrier height, giving a theoretical  $V_{\max}$  value well above the assumed value of  $\phi_b$ .

Owing to a calibration error on the indium oven in the MBE chamber, the first three samples (2781, 2787, 2792) were grown with an unknown indium mole fraction,  $y$ . That fraction was believed to be approximately 0.07 (35). After oven temperature calibration, similar samples were grown with the correct value for  $y$ .

Table IV. Pseudomorphic MODFET Growth Parameters.

Sample	$d_d$ (Å)	$t$ (Å)	$N_d$ (atoms/cm <sup>3</sup> )	$N_a$ (atoms/cm <sup>3</sup> )	$y$
2781	350	100	$2.5 \times 10^{18}$	$2.5 \times 10^{19}$	$\approx 0.07$
2787	350	75	$2.5 \times 10^{18}$	$2.5 \times 10^{19}$	$\approx 0.07$
2792	350	100	$3 \times 10^{18}$	$3 \times 10^{19}$	$\approx 0.07$
2812	350	100	$2.5 \times 10^{18}$	$2.5 \times 10^{19}$	0.15
2815	350	75	$2.5 \times 10^{18}$	$2.5 \times 10^{19}$	0.15
2816	350	100	$3 \times 10^{18}$	$3 \times 10^{19}$	0.15

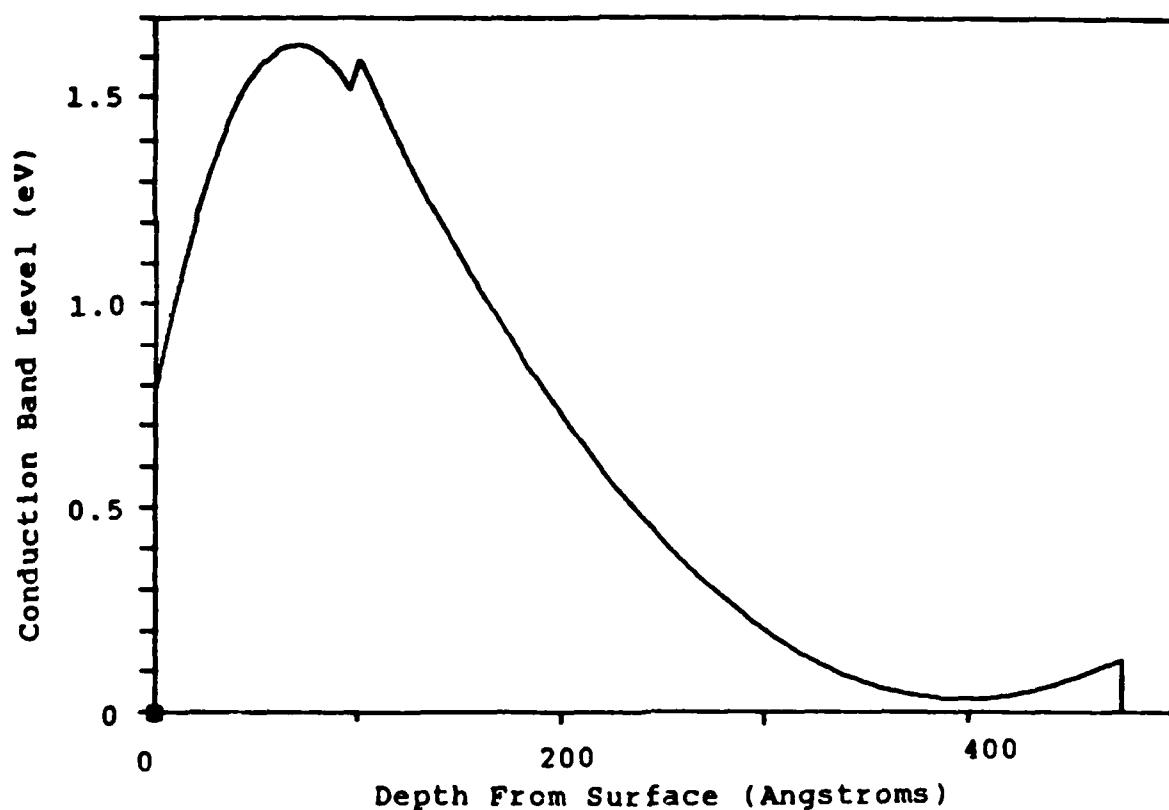


Fig 23. Computed Conduction Band Diagram for Device 2812.

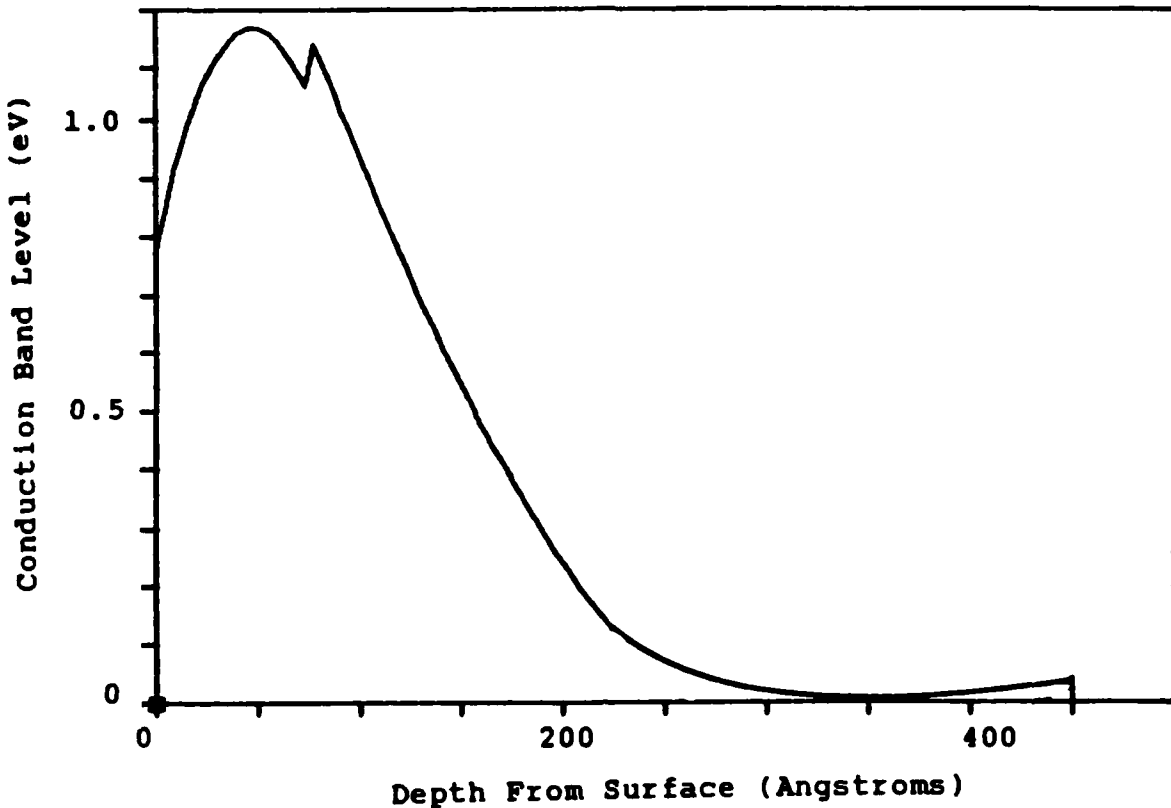


Fig 24. Computed Conduction Band Diagram for Device 2815.

#### Device Fabrication.

After crystal growth, the wafers were processed to produce individual MODFETs. All devices were fabricated with standard photolithographic techniques, using the MBE-grown wafers as the starting material. ES pseudomorphic MODFETs were fabricated both at the University of Illinois (UI) and at the Air Force Avionics Laboratory (AFAL), in separate processing procedures. Since the fabrication processes used at the two facilities are sufficiently different, they are described in detail in Appendices B and C, respectively.

The basics of the fabrication procedures will be described here. Similarities and differences of the two procedures will also be outlined.

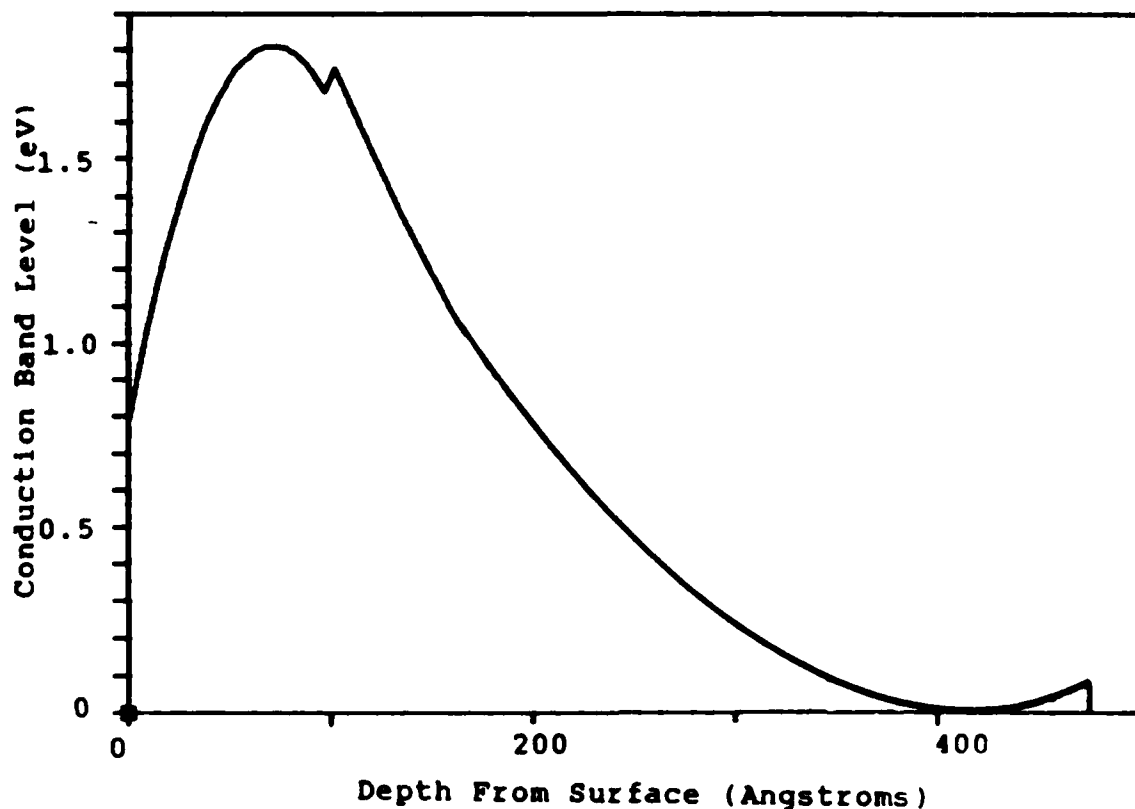


Fig 25. Computed Conduction Band Diagram for Device 2816.

Fabrication Procedure. After MBE growth, the wafer was cut into smaller chips for FET fabrication. To hold the wafers on mounting blocks in the MBE system, indium had been melted on the back of the wafer. Before device fabrication began, that indium on the backside was removed by etching to provide a relatively smooth back surface. Smoothness was



necessary for lithographic mask alignment and for tight vacuum when held in a photoresist spinner.

Actual fabrication at both facilities began with mesa etching. Photoresist was spun onto the surface and baked. The wafer was exposed under a mesa etch mask. After developing, exposed areas were etched away in a bath of dilute hydrofluoric acid (HF) and hydrogen peroxide ( $H_2O_2$ ). Wafers were etched down to the semi-insulating substrate. Mesas of active material remained. On these, individual FETs were then fabricated. Additionally, test pattern mesas remained. These patterns were used later to determine the resistance of the ohmic source and drain contacts.

Source and drain ohmic contacts were formed on the mesas. A lift-off technique was used, followed by rapid transient alloying. To begin the procedure, photoresist was spun on and baked. The wafer was exposed under a second mask. After developing, windows were left in the photoresist where ohmic contacts were to be made. Contact metal was evaporated onto the surface (Fig 4). In lift-off, the metal was removed from areas where the photoresist was not exposed, leaving metal only where the windows had been opened. The contacts were made ohmic by the alloying step. The chip was placed in an oven at 425 or 500° C (depending on the laboratory) for a short period. This allowed the metal to diffuse into the active regions below the contacts, making them highly n-type.

At this point, each wafer was scribed into two pieces

and separated into control devices and ES devices. The  $p^+$ -layer on the control sample was etched with a diluted solution of ammonium hydroxide ( $NH_4OH$ ) and  $H_2O_2$ . This step was the most troublesome portion of the fabrication procedure, and is described in detail in the next section.

After the control sample was etched, Schottky barrier gates were evaporated on the control and ES devices, between source and drain contacts. The gate metal in use varied among samples, as will be shown later. As with source and drain contact formation, a lift-off technique was used. First, photoresist was spun on the surface and baked. Gate patterns were exposed under a third mask. After developing, gate metal was evaporated onto the surface. The metal was lifted off, leaving Schottky barrier gates between source and drain contacts.

The next step of the fabrication process was evaporating contact metal on the source, gate and drain contacts. This step provided a sufficiently thick metal pad for subsequent wire bonding. Again, a liftoff technique was used. After photoresist application and baking, the chip was exposed under a fourth mask. Windows were opened in the photoresist over previously metallized contacts. Thicker metal was then evaporated onto the surface and lifted off.

A final step in fabrication was etching the  $p^+$ -layer between source, gate and drain contacts. This was accomplished to eliminate a parasitic current conduction path in the  $p^+$ -layer. Using only the gate, source and drain metals

as a mask, the samples were placed in an etchant long enough to remove the layer. This left  $p^+$ -GaAs only directly under the gate contact of the ES device and in the alloyed (and compensated) ohmic contacts of both control and ES devices.

Procedural Differences. There were differences between the fabrication processes used at UI and the AFAL. Some of these differences were simply the result of different standard procedures and equipment. The UI fabrications were performed first. Some of the different AFAL procedures were a response to problems encountered in the UI fabrications.

The first difference was in mask sets used. UI used a split source pattern (Fig 26) with a nominally  $1.5\text{ }\mu\text{m}$  gate length and  $290\text{ }\mu\text{m}$  gate width. The mask set available at AFAL incorporated gates  $150\text{ }\mu\text{m}$  wide, and gate lengths of  $1.35$  and  $2.35\text{ }\mu\text{m}$  nominally, interspersed throughout the mask. Only the  $1.35\text{ }\mu\text{m}$  devices were tested in later steps. That mask set also contained a dual source as shown in Fig 27. Scanning electron microscope measurements verified the gate lengths.

Throughout the actual fabrication, there were significant differences in photoresists used, spinning speeds, spinning times, photoresist developers and development time.

At UI, source and drain contacts were evaporated in a sequence of a Au/Ge eutectic alloy, followed by Ni and Au. This eutectic was not available at AFAL. Therefore the sequence was Ni, Ge, Au, Ni and Au. Contacts were alloyed after evaporation.

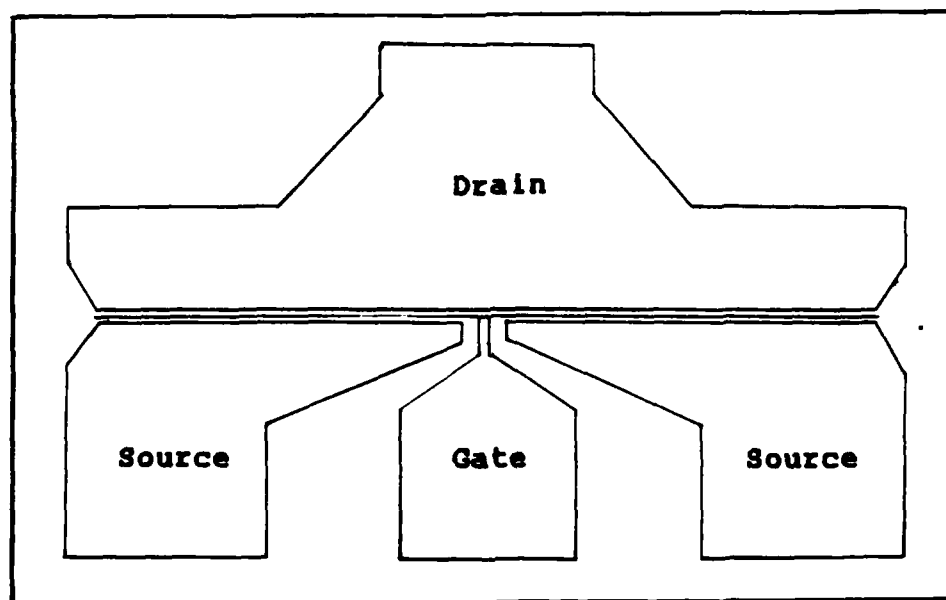


Fig 26. FET Mask Used at UI (2:29). The Mask Was Furnished by the Motorola Corporation.

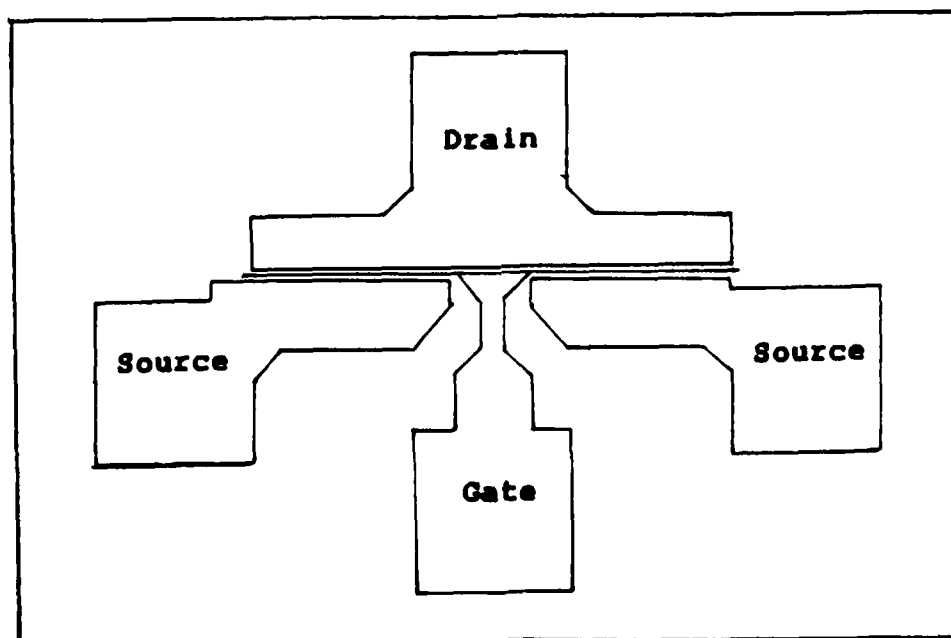


Fig 27. FET Mask Used at AFAL.

For most of the pseudomorphic MODFETs fabricated at UI, Al gates were used. After the fragility of the metal in later etching steps was determined, a decision was made to switch to a Cr, Pd and Au sequence at AFAL. With only non-reactive gold exposed, these gates withstood the etching steps without damage.

Control Sample Etching. Another difference in fabrication procedures was in the method of etching the  $p^+$  layer from the control samples. The different methods used were in response to the inability to produce control samples with acceptable characteristics.

The first control samples fabricated at UI were etched with a solution of  $NH_4OH : H_2O_2 : \text{deionized water (DIW)}$ , 3:1:150, by volume. Pseudomorphic MODFET control samples 2781-1A, 2787-1A and 2792-1A were etched with this solution after source-drain metallization, but before gate photolithography. The source and drain metal acted as masks for the etchant. In this manner, the  $p^+$ -layer was etched in the entire channel between source and drain. Samples were placed in the etchant long enough to remove the 75 - 100 Å  $p^+$ -layer. An etch rate of 30 Å/sec was assumed (36). As will be shown in the next chapter, this etch procedure resulted in control samples with very poor source-drain current characteristics. The procedure was modified for the next set of devices, in hopes of producing improved control device characteristics.

Pseudomorphic MODFET control samples 2812-1A, 2815-1A and 2816-1A were etched with a different procedure. It was postulated that the etch attacked the ohmic contacts of the previous samples, degrading their characteristics. The etchant either removed the metal or etchant products contaminated the source and drain contacts. Therefore, for these samples, the same etchant was used, but in a different manner. After source-drain metallization and alloying, gate photolithography was performed. After gate patterns were exposed and developed, the etchant was applied to the chip. The  $p^+$ -layer was etched through the gate windows in the photoresist. The difference between this procedure and the previous one are illustrated in Fig 28. After etching, again assuming a 30 Å/sec etch rate, the gate metal was deposited. This procedure also resulted in control samples with degraded I-V characteristics, with only one exception, as will be shown later.

At this point, with only one acceptable control sample produced, a new etchant was identified. Samples etched at AFAL were subjected to a solution purported to remove GaAs at a rate significantly higher than that for AlGaAs (37). This etch, was also a solution of  $NH_4OH$ ,  $H_2O_2$  and DIW. While the previous etch was mixed by volume, this one was mixed according to its pH.  $H_2O_2$  was placed in a beaker, and DIW-diluted  $NH_4OH$  (15:1) was pipetted in to bring the solution pH to a value of 7.05. This etch was found to react at a significantly lower rate than the one mixed by volume.

The rate was approximately 15 Å/sec. Thus, it was easier to control the etch and successfully fabricate control samples. Fig 29 shows drain-source I versus V characteristics of a device before and after etching. The etchant apparently removes the  $p^+$ -layer, but does not degrade the current carrying capability of the channel, if properly controlled. Later experimentation found the etchant to work even more reliably when used in an ultrasonic bath. Based on the success of this method in etching under the gate contact, the same etchant was subsequently used to etch the  $p^+$ -region between source, gate and drain contacts.

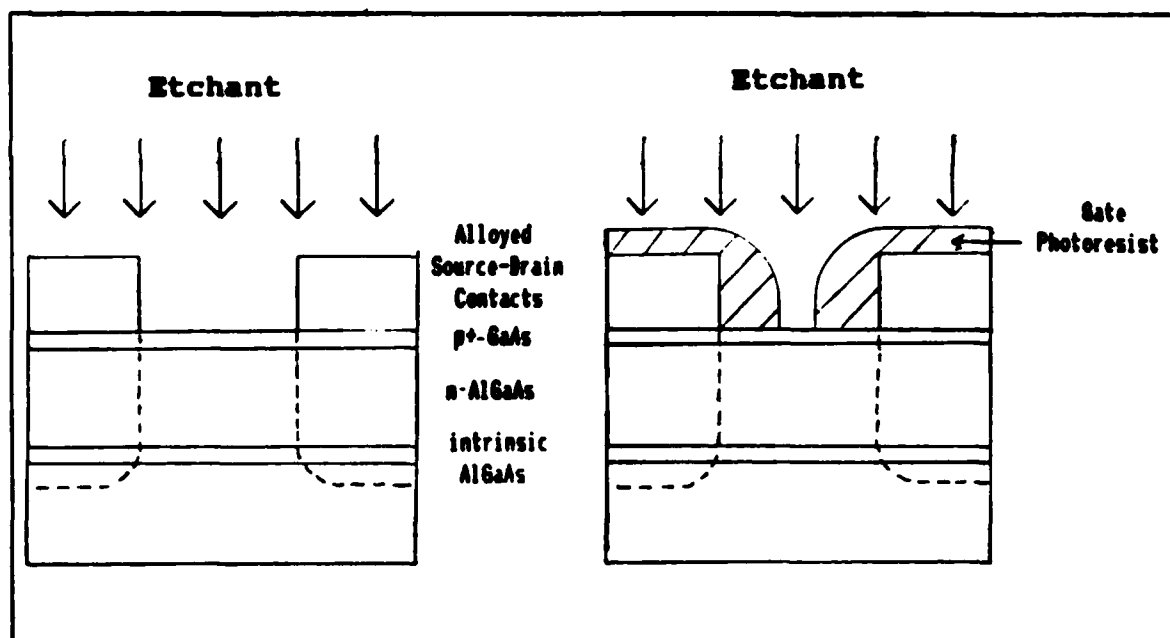


Fig 28. Methods of Etching  $p^+$  layer: (a) Etching in Entire Channel, Using Source and Drain Metal as a Mask and (b) Etching Through the Gate Window in Photoresist.

In summary, there were a number of differences in the way samples were fabricated. These are given in Tables V

and VI for UI and AFAL fabrications, respectively. Sample numbers reflect MBE growth numbers. Suffix numbers differentiate fabrication processes (-1 for UI fabrications, -2 for AFAL). Suffix letters define control (A) and ES (B) devices.

The success of the fabrication procedures and the variations in growth and processing were evaluated by a series of DC tests.

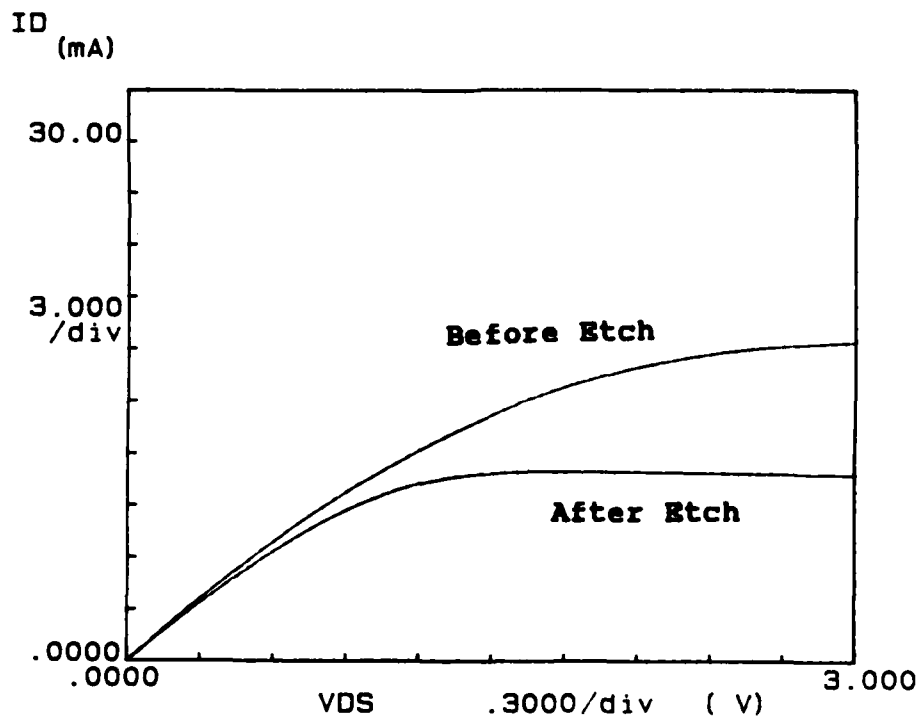


Fig 29. Device 2816 Drain-Source I versus V Characteristic (No Gate Contact Applied) Before and After Etching in pH 7.05.



Table V. Summary of UI Fabrication.

Sample	Type	Gate Metal	Control Sample p <sup>+</sup> Etch Method
2781-1A	Pseudomorphic	Al	Etch entire channel in 3:1:150
2781-1B	ES Pseudomorphic	Al	
2787-1A	Pseudomorphic	Al	As above
2787-1B	ES Pseudomorphic	Al	
2792-1A	Pseudomorphic	Al	As above
2792-1B	ES Pseudomorphic	Al	
2812-1A	Pseudomorphic	Al	Etch through gate mask, 3:1:150
2812-1B	ES Pseudomorphic	Al	
2815-1A	Pseudomorphic	Al	As for 2812-1A
2815-1B	ES Pseudomorphic	Al	
2816-1A	Pseudomorphic	Ti/Au	As for 2812-1A
2816-1B	ES Pseudomorphic	Ti/Au	

Note: -1 suffix denotes fabrication at UI. All control sample numbers end with 'A' and ES devices end with 'B'. All devices were fabricated with 1.5 x 290  $\mu$ m gates.

Table VI. Summary of AFAL Fabrication.

Sample	Type	Gate	Control Sample p <sup>+</sup> Etch Method
2781-2A	Pseudomorphic	Cr/Pd/Au	Through gate mask, pH 7.05, 15 sec
2781-2B	ES Pseudomorphic	Cr/Pd/Au	
2787-2A	Pseudomorphic	Cr/Pd/Au	As for 2781-2A
2787-2B	ES Pseudomorphic	Cr/Pd/Au	
2792-2A	Pseudomorphic	Cr/Pd/Au	As for 2781-2A
2792-2B	ES Pseudomorphic	Cr/Pd/Au	
2812-2A	Pseudomorphic	Cr/Pd/Au	Through gate mask, pH 7.05, 5 sec ultrasonic
2812-2B	ES Pseudomorphic	Cr/Pd/Au	
2815-2A	Pseudomorphic	Cr/Pd/Au	As for 2812-2A
2815-2B	ES Pseudomorphic	Cr/Pd/Au	
2816-2A	Pseudomorphic	Cr/Pd/Au	As for 2812-2A
2816-2B	ES Pseudomorphic	Cr/Pd/Au	

Note: -2 suffix denotes fabrication at AFAL. All control sample numbers end with 'A' and ES devices end with 'B'.

All devices were fabricated with 1.35 x 150  $\mu$ m gates.

#### DC Testing.

DC testing was used after source-drain metallization and annealing, and at the completion of the fabrication process.

After the ohmic contacts were formed, they were tested to determine their ohmic character. A standard transmission line method was used. A pattern of metallized contacts spaced at different intervals were driven with a current source, and the voltage drop between contacts measured.

Dividing the voltage by the driving current yielded the

combined resistance of the material and the 2 ohmic contacts. This was performed for several values of contact spacing. The resistances were plotted versus contact spacing. A linear regression method was used to draw a straight line through the data (Fig 30). The point where the line intercepted the resistance axis was the resistance of the two ohmic contacts. Half that value gave the resistance of one contact. Multiplying by the contact width gave normalized contact resistance in  $\Omega$ -mm.

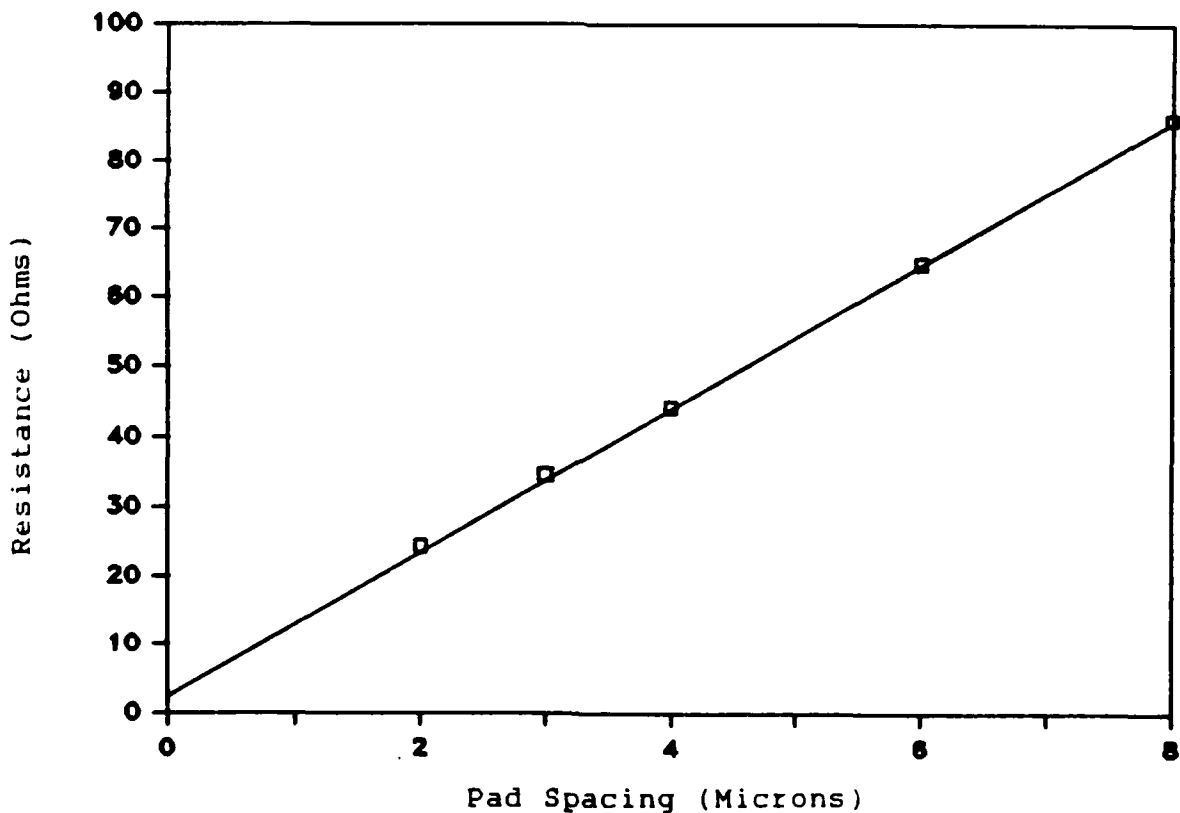


Fig 30. Plot of Resistances From TLM Patterns for Device 2812-2. The y Intercept is Twice the Value of the Contact Resistance.

Table VII lists experimental values for normalized contact resistance for several pseudomorphic samples. Since the measurement was made before control sample etching, only one result is given for each sample. Results for samples 2781-2, 2787-2 and 2792-2 must be treated as suspect. These samples exhibited significant contact shrinkage after alloying, resulting in possibly erroneous values of contact spacing and therefore of contact resistance for those samples.

Table VII. Ohmic Contact Resistance Results.

<u>Sample</u>	<u>Contact Resistance (<math>\Omega</math>-mm)</u>
2781-1	0.38
2781-2	0.12
2787-1	2.15
2787-2	0.12
2792-1	0.64
2792-2	0.04
2812-1	1.47
2812-2	0.08
2815-1	2.17
2815-2	0.002
2816-1	1.09
2816-2	0.13

After fabrication was completed, devices were electrically characterized at DC. This characterization included drain current versus drain voltage characteristics, at several values of gate voltage. Gate voltage was stepped only to the point where gate leakage current just became noticeable. An example is given in Fig 31.

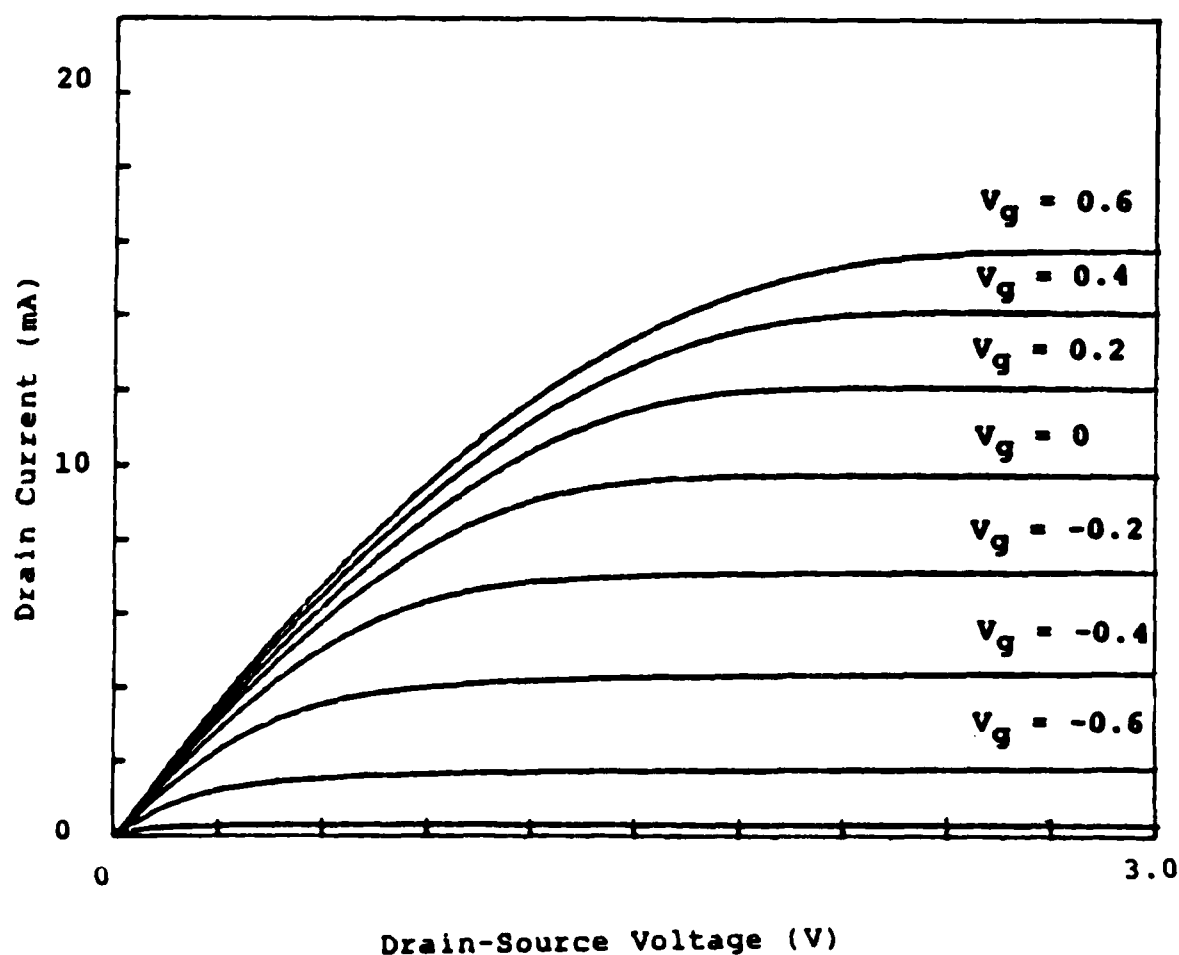


Fig. 31 Drain-Source I versus V Characteristic for Device

Source resistance ( $R_s$ ) was another DC measurement performed. The value of  $R_s$  is used later to determine intrinsic transconductance,  $g_{m0}$ . Using the scheme depicted in Fig 32,  $R_s$  could be determined directly. With a current source and voltmeter connected as shown, very little current flows through the drain resistance, owing to the high impedance of the voltmeter. Almost the entire voltage between drain and source is dropped at the source resistance. The value of  $R_s$  is then determined from Ohm's law. Values for  $R_s$  are given in Table VIII.

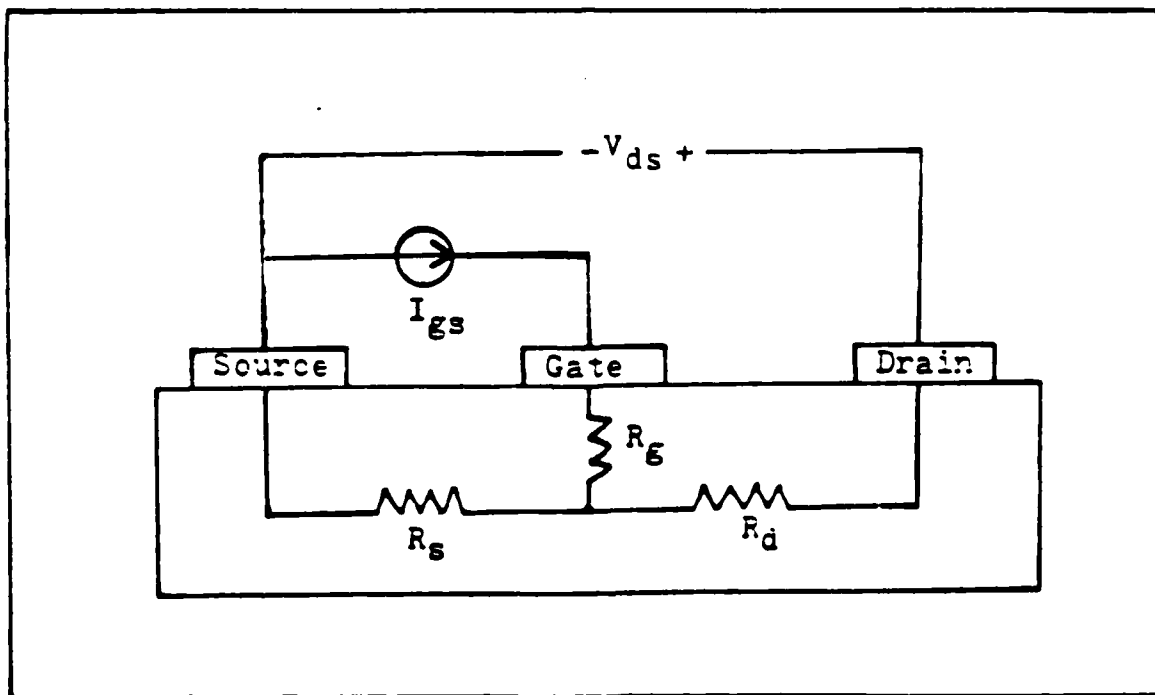


Fig 32. Circuit Diagram for Source Resistance Measurements (3:5-6).

Next, transconductance,  $g_m$ , was recorded over a range of gate voltages, along with drain-source current. Transconductance measurements were taken with  $V_{ds}$ , the drain voltage with respect to the source, set at 2.0 volts. The measured transconductance was calculated (in mS/mm) from:

$$g_m = \Delta I_d / \Delta V_g W \quad (21)$$

where  $\Delta I_d$  is a change in drain current (mA) with a change in gate voltage ( $\Delta V_g$  (V)) and  $W$  is the gate width in mm. The intrinsic transconductance ( $g_{m0}$ ) was then calculated from  $g_m$  and  $R_s$  using Eq 7. A typical plot is shown in Fig 33 with drain current versus gate voltage on the same plot. Peak  $g_m$  values observed for each device are given in Table VIII.

All devices which exhibited appreciable transconductance and drain-source current are shown.

Another parameter was determined from the plot of transconductance versus gate voltage. By drawing a tangent line to the transconductance curve as it rises above zero, the threshold voltage ( $V_{off}$ ) was determined. The point where that line intercepts the gate voltage axis is the value of  $V_{off}$ . Typical values are given in Table IX.

Also, gate current versus gate voltage was recorded, as shown for a typical case in Fig 34. Where the gate voltage began to rise linearly, a tangent line was drawn. The point where that line intercepted the voltage axis was designated as the barrier height. Ranges and mean observed values of barrier height are given in Table IX.

Table VIII. Source Resistance and Transconductance of Pseudomorphic Samples.

<u>Sample</u>	<u>R<sub>s</sub> (Ω)</u>	<u>g<sub>m</sub> (mS/mm)</u>	<u>g<sub>m0</sub> (mS/mm)</u>
2781-1A	-	-	-
2781-1B	9	150	246
2781-2A	20	150	272
2781-2B	23	120	204
2787-1A	-	-	-
2787-1B	0.5	110	110
2787-2A	0.1	250	250
2787-2B	11	160	221
2792-1A	-	-	-
2792-1B	1	160	168
2792-2A	-	-	-
2792-2B	4	160	178
2812-1A	15	40	48
2812-1B	14	126	278
2812-2A	14	200	343
2812-2B	13	190	296
2815-1A	10	92	127
2815-1B	14	140	315
2815-2A	14	230	453
2815-2B	13	220	383
2816-1A	12	148	297
2816-1B	12	122	216
2816-2A	12	220	366
2816-2B	11	200	297



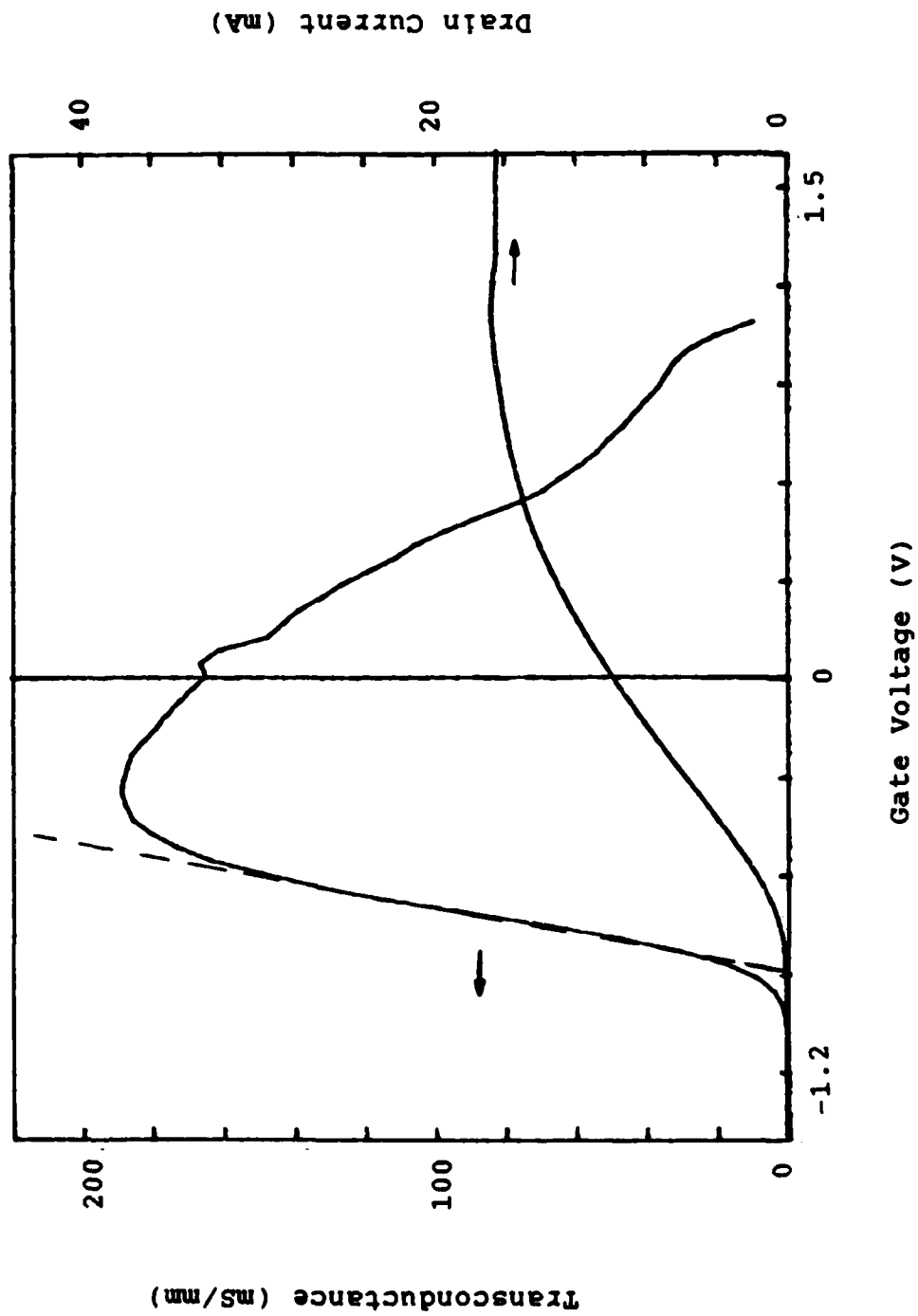
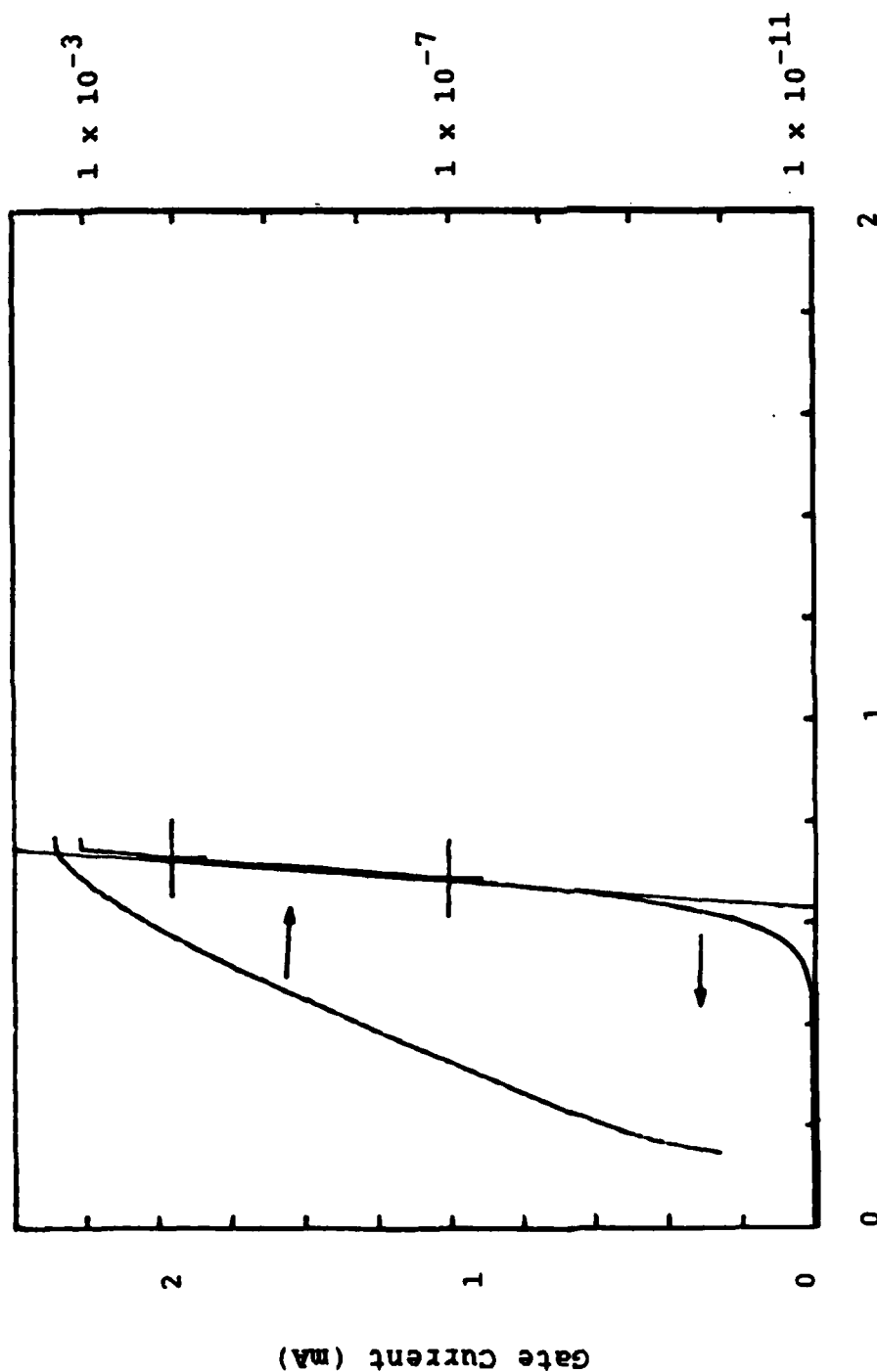


Fig 33. Transconductance and Drain Current Versus Gate Voltage for Device 2816-2B. The Tangent Line Gives  $V_{\text{off}} = -0.9$  V.  $V_{\text{ds}}$  Was Set to 2.0 V.



Gate Voltage (V)

Fig 34. Gate I versus V Curve for Device 2816-2B. The Tangent Line Shows  $V_{\max} = 0.63$  V.

Table IX. Threshold and Barrier Voltages for Pseudomorphic MODFETS.

Sample	$V_{\text{off}}$ (V)	Barrier Height	
		Mean	Range
2781-1A	-	1.14	1.02-1.35
2781-1B	-1.16	0.73	0.69-0.81
2781-2A	-0.15	0.71	0.59-0.78
2781-2B	-1.1	0.63	0.58-0.72
2787-1A	-	1.34	1.08-1.77
2787-1B	-0.56	1.38	1.20-1.48
2787-2A	-0.45	1.08	0.77-1.65
2787-2B	-1.1	0.83	0.57-0.98
2792-1A	-	1.38	0.85-1.64
2792-1B	-1.0	0.83	0.57-0.98
2792-2A	-	-	-
2792-2B	-1.9	0.87	0.69-1.09
2812-1A	-	0.93	0.75-1.04
2812-1B	-0.5	0.85	0.79-0.94
2812-2A	-1.1	0.72	0.63-0.72
2812-2B	-1.7	0.64	0.61-0.66
2815-1A	0.1	0.74	0.66-1.02
2815-1B	-0.9	0.88	0.83-1.04
2815-2A	-0.7	0.71	0.65-0.85
2815-2B	-1.1	0.61	0.56-0.66
2816-1A	-0.5	0.59	0.57-0.61
2816-1B	-1.3	0.56	0.54-0.59
2816-2A	-0.5	0.81	0.61-0.80
2816-2B	-0.9	0.62	0.58-0.68

A review of DC characteristics showed that only 5 samples met the established criteria for microwave testing (page 4-3). These samples had acceptable gain (transconductance) for both the ES and control samples. Samples 2787-2, 2812-2, 2815-2, 2816-2 and 2816-1 were identified for microwave testing.

#### Microwave Measurements.

Following complete DC characterization, the identified devices were tested at microwave frequencies. This process was performed to determine the relative high frequency performance of the ES devices against the control samples. Network analyzer measurements were performed first with devices on a wafer. An attempt was then made to dice and mount individual devices in microstripline packages for NF measurement.

Network Analysis. Equipment for network analysis is described in Chapter 3. Measurements were taken over the range of 2-12 GHz at 500 MHz intervals. The upper limit reflects the limited bandwidth capability of the microprobe station. Before testing the devices at microwave frequencies, the analyzer was calibrated using procedures in reference (31). This daily procedure eliminated systematic errors in measurement. The calibration procedure quantifies these errors and removes their effects through software routines.

After calibration, the proper operation of the analyzer was verified. This was accomplished by measuring the re-

sponse of a known device, such as an impedance-matched, through-stripline. The example in Fig 35 shows a through response taken immediately after calibration. It reveals the calibration to be accurate and uniform across the measurement spectrum. Transmission is very high and reflection very low, as expected for a matched through line.

FREQUENCY MHz	REFL COEFF-IN S11		FORWARD-TRAN S21		REVERSE-TRAN S12		REFL COEFF-OUT S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2000.0000	.00	-96.25	1.00	.73	1.00	.77	.00	-95.39
2500.0000	.00	-126.45	1.00	.71	1.00	.70	.00	-125.47
3000.0000	.01	170.53	1.00	-.06	1.00	-.06	.01	162.69
3500.0000	.01	97.68	1.00	-.32	1.01	-.28	.01	106.74
4000.0000	.01	93.24	1.00	.73	1.00	.71	.01	92.56
4500.0000	.01	-21.80	1.00	.62	1.00	.64	.01	-22.51
5000.0000	.01	-68.56	1.00	.26	1.00	.25	.01	-68.44
5500.0000	.01	-122.51	1.00	.10	1.00	.09	.01	-123.40
6000.0000	.01	-151.62	1.00	.12	1.00	.11	.01	-151.12
6500.0000	.01	171.37	1.00	.64	1.00	.68	.01	170.26
7000.0000	.01	115.68	1.00	.44	1.01	.45	.01	115.86
7500.0000	.02	75.51	1.00	-.49	1.00	-.51	.02	77.79
8000.0000	.01	-4.66	1.00	-.44	1.00	-.45	.01	-5.46
8500.0000	.02	-30.37	1.00	-.29	1.00	-.25	.02	-31.46
9000.0000	.03	-78.92	.99	-.27	.99	-.26	.03	-80.43
9500.0000	.05	-142.09	1.01	.10	1.01	.10	.05	-142.30
10000.0000	.05	-178.55	1.01	-.74	1.01	-.70	.05	-179.43
10500.0000	.08	73.96	.98	-2.27	.98	-2.30	.08	73.95
11000.0000	.11	59.31	1.00	-2.67	1.00	-2.69	.11	59.32
11500.0000	.13	-4.25	.97	-4.40	.97	-4.40	.13	-4.65
12000.0000	.33	-65.06	.88	-7.38	.88	-7.35	.34	-65.54

Fig 35. Calibration Data for a Through Stripline.

Actual network analysis measurements were then taken. The device under test was then placed in the system and DC biased for maximum forward gain ( $s_{21}$ ). This DC bias point was consistently at a higher gate voltage for control samples. The analyzer was swept over the range of 2-12 GHz by computer control. The analyzer recorded all S-parameter responses. After the measurement was completed, the results were tabulated. A typical tabulated response is given in Fig 36.

From the network analyzer data,  $f_{\max}$  and  $f_T$  were determined

from calculations of the maximum power gain,  $G_{A,max}$  and the forward current gain of the device,  $h_{21}$ . From (38),

$$G_{A,max} = \left| \frac{s_{21}}{s_{12}} K \pm (K^2 - 1)^{1/2} \right| \quad (22)$$

$$\text{where } K = \frac{1 + |s_{11}s_{22} - s_{11}s_{21}|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{12}s_{21}|}$$

and

$$h_{21} = \frac{-2s_{21}}{(1 - s_{11})(1 + s_{22}) + s_{12}s_{21}} \quad (23).$$

The parameters  $s_{11}$ ,  $s_{21}$ ,  $s_{12}$  and  $s_{22}$  have their standard definitions (38).

2816-1A 7 11 VG=0.37 ID=19 MA									
FREQUENCY MHz	REFL COEFF-IN S11		FORWARD-TRAN S21		REVERSE-TRAN S12		REFL COEFF-OUT S22		
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	
2000.0000	.53	-85.68	4.36	115.26	.02	-23.14	.61	-13.81	
2500.0000	.36	-82.46	3.23	106.24	.00	-70.27	.62	-10.35	
3000.0000	.35	-80.04	2.62	107.87	.00	36.89	.64	-12.63	
3500.0000	.39	-88.22	2.50	107.24	.01	7.24	.63	-16.59	
4000.0000	.40	-100.36	2.37	102.18	.02	-14.11	.61	-18.88	
4500.0000	.37	-110.51	2.14	99.86	.02	-34.62	.59	-19.98	
5000.0000	.34	-119.07	1.95	94.16	.03	-53.49	.58	-20.51	
5500.0000	.30	-124.05	1.75	93.35	.03	-63.14	.58	-21.70	
6000.0000	.28	-123.17	1.58	90.67	.03	-75.02	.58	-22.43	
6500.0000	.28	-123.23	1.41	89.62	.02	-79.45	.59	-23.52	
7000.0000	.27	-126.07	1.33	87.72	.03	-84.91	.58	-25.38	
7500.0000	.27	-128.49	1.27	85.35	.03	-88.58	.58	-25.97	
8000.0000	.27	-130.85	1.19	86.68	.03	-91.87	.57	-28.06	
8500.0000	.26	-132.51	1.11	80.63	.03	-99.80	.58	-26.70	
9000.0000	.24	-130.21	1.02	80.10	.03	-99.81	.59	-26.15	
9500.0000	.27	-122.67	.99	81.87	.03	-101.35	.64	-28.09	
10000.0000	.35	-123.62	.93	83.28	.03	-108.63	.66	-32.94	
10500.0000	.42	160.38	1.04	70.12	.04	-95.72	.64	-40.17	
11000.0000	.22	166.57	.86	71.41	.03	-109.05	.56	-33.28	
11500.0000	.12	-139.48	.81	77.11	.03	-114.66	.65	-39.95	
12000.0000	.25	-106.77	.85	71.99	.03	-122.00	.75	-60.17	

Fig 36. Sample Output Data From Network Analyzer Measurements.

The values of  $G_{A,max}$  and  $h_{21}$  are plotted on a log-linear scale for each measured ES pseudomorphic MODFET and control sample (Appendix D). A line is drawn through the data and the point where  $G_{A,max}$  falls to 0 is  $f_{max}$ . The value where  $h_{21}$  falls to 0 is  $f_T$ . Tabulated values are given in Table X.

Table X. Microwave Response Data.

<u>Device</u>	<u><math>f_T</math> (GHz)</u>	<u><math>f_{max}</math> (GHz)</u>
2787-2A	10.8	15.0
2787-2B	9.6	12.2
2812-2A	10.5	12.2
2812-2B	10.1	11.2
2815-2A	14.8	17.5
2815-2B	10.7	12.2
2816-2A	12.7	16.0
2816-2B	8.0	10.5
2816-1A	10.0	11.1
2816-1B	8.4	9.2

Lapping and Dicing. To make noise figure measurements on individual devices, it was necessary to lap wafers to approximately 200-250  $\mu$ m thickness. Next, wafers had to be diced into individual devices for mounting into the micro-strip package of Fig 21.

To thin the wafers, they were placed transistor-side down on a glass slide and mounted there with wax. The substrates were then mounted in a jig and thinned on a

lapping table. After demounting and cleaning, the wafers were DC tested to verify that lapping did not damage the devices.

Next, wafers were diced into discrete devices. They were mounted on a sheet of sticky plastic film and diced using a wafer saw. During the cutting operation, DIW was sprayed on the surface to cool and wash the wafer. DC tests were again performed on the devices to verify proper operation before bonding into a microstripline package. Unfortunately, testing at this stage revealed significant, almost total degradation of DC characteristics. Transconductance and drain current were typically less than 1% of their values before dicing. A device that exhibited a peak current of 25 mA before dicing could only produce 400  $\mu$ A after. That degradation made it impossible to proceed with the intended noise figure measurements.

Despite the absence of NF data, it was still possible to analyze the success of the experiment, based on DC and network analyzer data. This analysis is presented in the following Chapter.



## V. Analysis of Results.

As the results of Chapter 4 show, the Schottky barrier height was not raised for the pseudomorphic MODFET with a surface  $p^+$ -layer under the gate. In this chapter, possible causes of that discovery will be postulated. Other results for the ES device will also be compared and contrasted to those for their respective control samples. These include transconductance, threshold voltage, contact resistance and microwave response. Finally, the fabrication processes used in this effort will be discussed and their impact on the results analyzed.

### Schottky Barrier Height

The computer-generated plots of Figs 23, 24 and 25 suggest that the ES pseudomorphic MODFET samples should exhibit barrier height increases of between 0.4 and 0.8 V over their respective control samples. The experimental barrier height data in Table IX, however, indicate that the Schottky barrier for the ES device did not increase. Both the mean observed barrier height and the minimum and maximum observed barrier heights for the control samples were higher than those for the corresponding ES sample. These observations are summarized in Fig 37, where the predicted ES pseudomorphic MODFET conduction band, the pseudomorphic MODFET conduction band, and an estimate of the conduction band based on observed data are given. There was only one

exception to this trend of lower Schottky barriers on ES devices. On sample 2815-1, the mean and range values for the ES device slightly exceeded those for the control sample. Since the sister sample, 2815-2, did not exhibit the same behavior, this is probably not a result of the phenomenon of concern here. Rather, it is likely a result of an unknown processing variable.

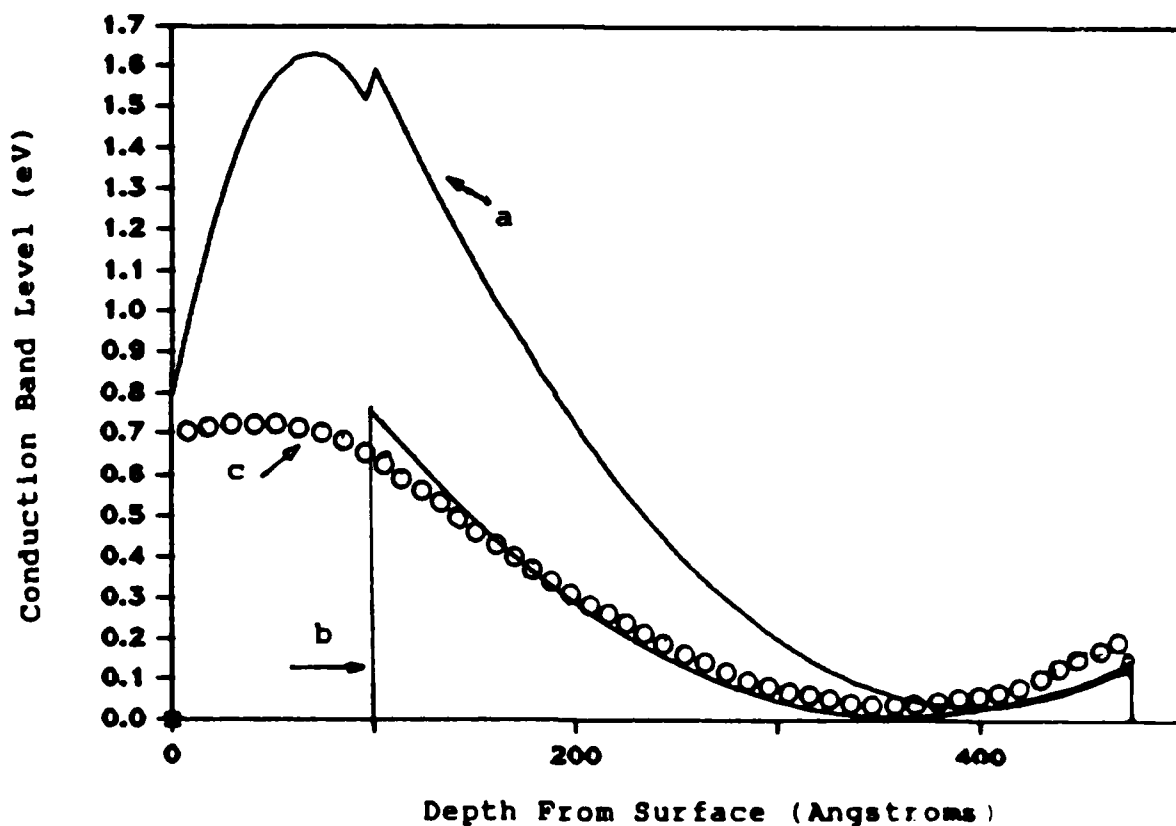


Fig 37. Pseudomorphic MODFET Conduction Band Diagram (a) ES Device (Calculated) (b) Control Device (Calculated) and (c) ES Device, Based on Observed Data

This surprising trend of lower barriers may be the result of different phenomena. The explanations postulated here are highly speculative.

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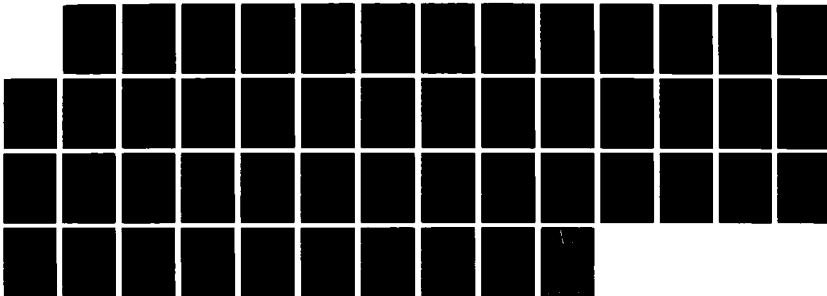
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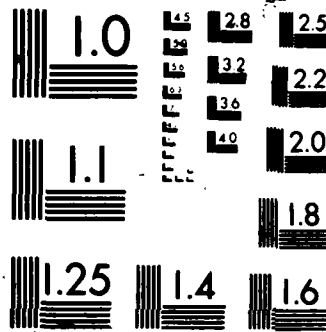
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avenues of exploration in attempting to increase ES barrier heights. The possibilities include problems with the incorporation of Be atoms in the GaAs lattice during MBE growth, the incorrect adaptation of the ES MODFET theory of reference (3), and excess strain in the lattice of the pseudomorphic structure. The possibility that the  $p^+$  layer was etched during fabrication was also considered.

It is conceivable that the surface GaAs layer was not doped properly during MBE growth, or that the Be dopant atoms diffused out of the GaAs layer at some later stage in processing. The layer was grown with a substrate temperature of  $610^\circ\text{C}$  (36). The only other time during fabrication that the wafer was at an elevated temperature was during ohmic contact alloying, when the temperature was  $500^\circ\text{C}$  (UI) or  $425^\circ\text{C}$  (AFAL), both for periods less than one minute. There is no appreciable diffusion of Be atoms at these temperatures and times (39). A concentration-dependent diffusion coefficient of  $10^{-16} - 10^{-15}\text{ cm}^2/\text{sec}$  has been reported for  $2-3 \times 10^{19}\text{ cm}^{-3}$  Be atoms in GaAs at  $600^\circ\text{C}$ , but the coefficient rises quickly to  $10^{-12}\text{ cm}^2/\text{sec}$  for  $N_A = 5 \times 10^{19}\text{ cm}^{-3}$  (40). Additionally, Be atoms have been observed to rapidly and anomalously diffuse interstitially during MBE growth at  $680^\circ\text{C}$ , converting adjacent semi-insulating GaAs into  $p^+$ -GaAs (41). This occurs for Be concentrations above  $1 \times 10^{19}\text{ cm}^{-3}$  (41:4131). If interstitial Be atoms were available in the GaAs layer, this same mechanism could conceivably result in Be diffusion into the n-type AlGaAs of

the ES pseudomorphic MODFET and compensation of the Si dopant atoms. This would result in a lower conduction band level and therefore a lowered barrier height. For the control samples, the compensated AlGaAs region would probably have been etched with the  $p^+$  layer. It is also possible but less likely that Be atoms precipitated out of the lattice, forming oxides at the surface or disrupting the AlGaAs interface.

Another possible explanation for the lower barrier heights on ES pseudomorphic MODFETs lies in the theory developed for barrier enhancement. Priddy (3) performed his analysis on standard MODFETs, beginning with the conduction band structure of Fig 7. The quantum well of the pseudomorphic MODFET (Fig 18) is significantly different; there is a second band discontinuity where the InGaAs layer meets the GaAs buffer layer, resulting in a rectangular quantum well rather than the triangular one of the standard MODFET (Fig 7). There is also a different conduction band offset,  $\Delta E_c$ , at the InGaAs/AlGaAs interface, owing to the fact that this structure uses a different Al mole fraction  $x = 0.15$ . The InGaAs/AlGaAs quantum well is also deeper than that for GaAs/AlGaAs by approximately 300 meV (35). There may be enough perturbation of the band structure due to these differences that the ES MODFET charge control model no longer holds in its present form, or at best provides only a qualitative prediction of the barrier height.

Yet another phenomenon may cause the lower barrier in

the ES pseudomorphic MODFET. As stated earlier, there is a lattice mismatch at the interface of the InGaAs layer with the GaAs buffer layer below and the AlGaAs layer above. That strain may carry through the AlGaAs layer into the  $p^+$ -GaAs cap. As the total AlGaAs and  $p^+$ -GaAs thicknesses increase, so does the amount of strain (42). That strain would affect the barrier height. The total thickness of material above the InGaAs layer is 455 - 480 Å for devices fabricated in this effort. No other pseudomorphic device has been grown with such a large epitaxial thickness. Since the control samples had some of that thickness etched away, the lattice of those devices would experience less strain and less band bending, resulting in a higher barrier. Current theoretical efforts at the University of Michigan are addressing this possibility of increased strain using computer simulations (42).

Analysis of the barrier height data also reveals that the barrier height is fabrication dependent. The barrier height data in Table IX indicates that, in most cases, UI and AFAL fabrications do not result in the same mean and range of barrier heights. There is no trend, however, to indicate that the UI devices (those with a -1 suffix) are consistently higher or lower than the AFAL devices (-2 suffix). No conclusive explanation for this phenomenon can be offered. However, analysis of the gate metals used for each sample (Tables V and VI) shows that those with Al as the gate metal exhibit higher barriers than those with

Cr/Pd/Au. The one sample with the Ti/Au gate (2816-1) reveals a lower barrier than all others.

It should also be noted that there is as much variation in barrier heights from one fabrication to another as there is from ES device to control sample. Additionally, in some cases there is a large range of observed barrier heights across an individual sample. These observations may be attributable to arsenic oxide formation under the gate metal in some cases, even though the native surface oxides on GaAs are unstable (43). It is also possible that beam flux and doping variations across the wafer during MBE growth contributed to the observed variations in barriers (3:6-4).

Another possible explanation for the barrier height observations is that the  $p^+$ -layer was etched at some point during fabrication. That eventuality was discounted for two reasons. Extreme care was taken during fabrication to ensure that no etchants came in contact with the  $p^+$ -layer under the gate region. The only substances with which the surface came in contact were DIW and organic solvents such as trichloroethane, acetone, and methyl and isopropyl alcohols. Because of the possibility of surface etching, the wafer was not exposed to DIW for long periods, and no ultrasonic agitation of the wafer was allowed during fabrication. Additionally, had the surface been etched, the gate metal would have been evaporated onto the n-type AlGaAs, resulting in barrier heights nearly identical to those of the control samples, instead of the lower barriers observed.



In addition to the barrier height, there are other experimental results that are worthy of note. These include transconductance, contact resistance, threshold voltage and microwave response.

### Transconductance

From Table VIII, it is evident that control samples exhibit a higher transconductance in all cases. This correlates with the transconductance expressions, Eqs 6 and 12. For the ES device, the spacing between gate metal and the 2DEG is greater than for the control sample. One then expects a lowered transconductance for the ES device. This may be described as a disadvantage. The fact that the gate cannot be recessed because of the presence of the  $p^+$ -layers means that it is not possible to realize very high transconductances, using these fabrication techniques. This may be overcome with a method using a  $p^+$ -implantation into a recessed gate region.

Another comparison may be made between the best observed value of external transconductance (230 mS/mm for sample 2815-2A) and the best result reported in literature for a comparable device (270 mS/mm) (6:567). It should be noted that the best reported device used a 1  $\mu$ m gate length and 100 Å recessed gate, while device 2815-2A utilized a 1.35  $\mu$ m gate and no gate recessing. Considering these limitations, the values obtained here are quite remarkable.

### Contact Resistance

The data of Table VII show that there was a great deal of variation in contact resistance from sample to sample and between fabrications. The UI fabrications produced a wide variation in contact resistance, while the AFAL results were consistently low. The best contact resistances observed ( $0.002 \text{ } \Omega\text{-mm}$  for device 2815-2) are better than the best ohmic contacts reported in the literature (44), which were as low as  $0.035 \text{ } \Omega\text{-mm}$ . These low contact resistances contribute to the high transconductance observed earlier.

The consistently low AFAL resistances can probably be attributed to the equipment used. The AFAL alloying procedure was performed with a computer controlled oven. That closed-loop system provided precisely controlled alloying temperatures and times. Once the procedure was started, no operator intervention was required. At UI, on the other hand, the alloying procedure was completely manual.

The source-drain metal depositions may also have affected the results. Different metal layerings were used at the two laboratories (see Appendices B and C). Contacts are made ohmic by alloying due to the diffusion of Ge atoms from the surface deposition. Perhaps atoms diffused more readily from the discrete Ge layer used at AFAL than from the Au/Ge eutectic used at UI, resulting in higher concentrations at the contact and less resistance.

### Threshold Voltage

From Table IX, the threshold voltage,  $V_{\text{off}}$ , is lower for the ES device than the control sample, making the ES device more depletion mode than the control sample. This is observed in all seven cases where data are available. Those control samples where no value of  $V_{\text{off}}$  is given are those where no appreciable transconductance was observed, due to overetching. The expression for  $V_{\text{off}}$  in an ES MODFET, Eq 9, does not predict this lower ES device value. However, Eq 2, which gives the threshold voltage for a standard MODFET, was an adequate predictor of the change. That equation predicts that  $V_{\text{off}}$  will decrease with increasing doped AlGaAs thickness. Since the  $p^+$ -layer effectively adds to that thickness, one may surmise that the results of this effort are not inconsistent with that model. The resulting change in  $V_{\text{off}}$  from control to ES devices is relatively constant across the sample set, ranging from 0.4 to 0.8 V. Three samples fabricated and etched together late in the effort; 2812-2, 2815-2 and 2816-2; exhibited a more consistent change in  $V_{\text{off}}$ . This points to the variations in etchants and etch procedures as a primary cause for the variable change in  $V_{\text{off}}$ . The change in  $V_{\text{off}}$  could probably be made more consistent with additional experiments, since the optimal and most consistent etch procedure was found late in the effort.

### Microwave Response

As the data in Appendix D and Table X indicate, control sample microwave responses consistently surpass those of ES devices. Analysis did not predict this result (Eq 14), but suggests equal responses. An explanation may be gleaned from the results of previous work. It has been observed that gate-source capacitance ( $C_{gs}$ ) is often a function of gate bias, decreasing linearly with increasing gate voltage, even in regimes where transconductance is relatively constant (45:784). In this effort, to obtain maximum forward gains, the control samples were biased at higher values of gate voltage than were the ES devices. If the capacitance in fact decreased with increasing gate voltages, the higher gate bias would result in the improved microwave responses.

Previous efforts have also indicated that placing the gate metal closer to the 2DEG improves switching speed of the device (12:1020). This is attributed to parasitic interconnect capacitances. As the gate is recessed, the transconductance increases, as well as the capacitance between the gate finger and the source contact ( $C_{gs}$ ). However, if the parasitic interconnection capacitances are significantly larger than that intrinsic capacitance, the effect of recessing has a minimal effect on overall capacitance. Such may be postulated as the effect observed here. The control devices, by virtue of the  $p^+$ -layer etching, effectively incorporate a "recessed" gate, compared to the ES devices. This results in the higher transconductance with

little change in total capacitance. The result is improved microwave performance.

Again, the devices produced in this effort are qualitatively comparable to those cited in published literature (6). Device 2815-2A exhibited an  $f_T$  of 14.8 GHz and  $f_{max}$  of 17.5 GHz, while for the  $y = 0.15$  device in ref (6),  $f_T$  was 21.5 GHz and  $f_{max}$  was 37.0 GHz. One cause of the difference is extracted from Eq 15. Had a 1  $\mu\text{m}$  gate length ( $L_g$ ) been used instead of the 1.35  $\mu\text{m}$  gate, an increase in  $f_T$  of 35% could be expected, yielding a 20 GHz cutoff. A similar improvement in  $f_{max}$  could also be expected. Additionally, in the published results, the gate was recessed approximately 100 Å more than in this effort. Likely, this would result in higher transconductance and improved high frequency performance, as discussed in the preceding paragraph.

In summary, the degraded performance of the ES pseudomorphic MODFET as compared to the control samples can be attributed to one primary cause. The additional thickness of the  $p^+$ -layer moves the gate further away from the 2DEG, resulting in lower values of threshold voltage, transconductance and peak microwave operating frequency. While it is not certain that the  $p^+$ -GaAs layer was etched completely, it is known from the results that the control sample etch procedure removed the layer at least partially. There is certainly a smaller gate-2DEG distance on the control samples. All the observed differences between control and ES devices (except the lower ES barrier) can be attributed to

the greater gate-2DEG distance of the ES device, not to the  $p^+$ -doping of the layer. Why the  $p^+$ -layer had no effect was discussed earlier in this chapter.

One final analysis examines the fabrication procedures used in this effort.

#### Fabrication Procedures.

Two primary fabrication procedures at two different laboratories were used in this effort, using significantly different equipment and operating procedures, although the basic fabrication technology was the same. Within this framework, a number of variations were integrated. There were different device doping levels and layer thicknesses. Different gate metals were used and varying etch procedures were attempted. A total of 24 different samples were fabricated from 6 MBE growths using a variety of FET fabrication procedures, in which every effort was made to protect the integrity of the  $p^+$ -layer. The results were relatively consistent across the range of samples. Had there been any errors in fabrication that resulted in lowered barrier heights for the ES samples, it is highly unlikely that the error would be repeated across so broad a range of fabrication conditions.

If there are factors in the ES pseudomorphic MODFET fabrication process that led to unexpected results, they must be in the general method for growth, fabrication and etching. Perhaps the wet chemical etch procedures used to remove the  $p^+$ -layer somehow alter the characteristics of the

device. With this method, it is very difficult to predict and control the rate at which the  $p^+$ -layer is etched. At these small dimensions, it is even more difficult to assess directly exactly how much material has been etched. It was impossible to determine exactly when the layer had been completely etched and when the removal process should be stopped to prevent the etching of the underlying AlGaAs layer.

It is also possible that the thin  $p^+$ -GaAs layer is somehow damaged by the multitude of processing steps the wafers must go through before the gate contact is applied. With the  $p^+$ -layer as thin as it is, it would not be difficult to damage or remove the layer in handling, cleaning and processing. There is even the possibility that the photoresist developing chemicals can etch GaAs, although the rate of etching is not known.

## VI. Conclusions and Recommendations

The pseudomorphic MODFET is a device which has the potential of revolutionizing the semiconductor industry, owing to its extremely high electron mobility and carrier saturation velocity. This thesis has contributed to the development of that device by investigating variations of its structure. The impacts of these variations were measured at DC and microwave frequencies. There are consistent, reproducible and significant consequences to report. These results are summarized in the following conclusions. Recommendations for future study of the device and its processing procedures complete the discussion.

### Conclusions

1. Pseudomorphic and ES pseudomorphic MODFETs were successfully fabricated from the same MBE-grown wafers, using identical fabrication processes. Fabrication in different laboratories yielded similar results. The  $p^+$ -layer on the control samples was etched before deposition of the gate contact.
2. The samples exhibited extremely low contact resistances, as low as  $0.002 \Omega\text{-mm}$ . These values are comparable to or better than the best reported values for this family of devices.
3. Extremely high transconductance values were ob



served, as high as 230 mS/mm at room temperature. These values are exceptional for devices fabricated with 1.35 - 1.5  $\mu\text{m}$  gate lengths and no gate recessing.

4. The devices exhibited microwave responses as high as 15-17 GHz. Considering the large gate lengths used, the values are comparable to the best microwave responses reported in the literature.

5. Pseudomorphic MODFETs fabricated without  $p^+$ -layers under the gate contact consistently exhibited higher Schottky barrier heights than those with the layer. This result was unexpected, since the charge control model developed in ref (3) predicted a larger barrier for the ES device.

6. The reduced barrier height of the ES pseudomorphic MODFET may result from one of three physical mechanisms. The Be dopant atoms may not have been incorporated into the lattice properly. The physical differences between standard and pseudomorphic MODFETs, which are not taken into account in the charge control model, may contribute to errors in the model. Lattice strain in the pseudomorphic MODFET may limit the barrier height.

7. The wet etching procedures were difficult to use, apparently etching faster than published rates. The pH 7.05 etch was found to react sufficiently slow to preserve device characteristics, while removing the  $p^+$  layer in reasonable time periods. Etching in an ultrasonic bath apparently makes the etch depth more reproducible. This is

probably because the bath breaks surface tension in the very small etch channels, and keeps fresh etchant on the wafer surface.

8. Control samples consistently exhibited higher transconductance and microwave response than ES devices. This is directly attributable to the smaller distance between the gate and 2DEG. This may be a significant disadvantage to the use of enhanced Schottky devices fabricated with the methodology used here. The use of  $p^+$ -doped surface layers produces a penalty in DC and microwave response.

9. The ES pseudomorphic MODFETs were more depletion mode than their reference counterparts. This also is attributable to the greater distance of the gate from the 2DEG. Consequently, this may limit the range of applications for the device.

10. Using a wafer saw to dice samples resulted in the degradation of device characteristics. That may be caused by the process itself, or the process may impact the integrity of the strained lattice of the device.

#### Recommendations

The following recommendations for future investigation are based on the results outlined above. The investigations suggested should be of great significance as this important pseudomorphic device is further developed.

1. Fabricate ES pseudomorphic MODFETs with lower doping in the  $p^+$ -layer. This may produce higher barriers on the ES devices, especially if the incorporation of Be atoms in the

lattice is a significant factor.

2. Attempt the MBE growth with the AlGaAs gradually graded down to GaAs under the  $p^+$ -layer, instead of the abrupt change used in this effort. This would alter the band structure of the device, possibly allowing the  $p^+$ -layer to enhance the barrier. It would indicate whether there are additional factors that should be incorporated in the charge control model to accurately predict barrier heights on ES pseudomorphic devices.

3. Attempt ES device fabrication with AlGaAs layers as thin as 250 Å and  $p^+$  GaAs layers as thin as 50 Å. This may reduce lattice strain and contribute to higher barriers, while retaining the essential elements for MODFET operation.

4. Investigate the actual etch rate of the pH 7.05 etchant on very thin films. All data published on the etchant to this point has concentrated on etching of bulk GaAs and AlGaAs. Precise data on etching of thin films would indicate exactly how long is required to etch the  $p^+$ -layer without removing the underlying AlGaAs.

5. Attempt  $p^+$  layer etching with alternate dry etching techniques. Reactive ion etching may be a suitable candidate, since it etches very isotropically and to precise depths.

6. Investigate an implantation technique for establishing a  $p^+$ -layer under the gate. Such a technique could raise the barrier, while keeping the gate metal close to the 2DEG, minimizing penalties in transconductance and microwave

response.

7. Investigate the problem of dicing individual devices from the wafer. Determine if degradation was due to impurities in the DIW used in dicing, or if vibrations from the wafer saw contributed to the degraded characteristics. If vibration caused the degradation, that would significantly impact the feasibility of using pseudomorphic MODFETs in a range of practical applications.

8. Develop a more exact treatment of the charge control model for this device. Perform a review and update of the ES MODFET theory to incorporate the different structure, quantum well and conduction band of the pseudomorphic MODFET.

APPENDIX A

Band Diagram Modelling Program

```

100 '***** PSEUDO-MORPH PLOT PROGRAM *****
****
110 ' Revised and corrected 4 April 1986
120 ' Written by Kevin L. Priddy
130 ' This program plots the band diagram given Na, Nd, Vb,
x, and the layer thi
cknesses
140 ' Program to determine Ns and Voff and plot the band dia
gram.
150 ' This program assumes the depletion approximation is va
lid and also puts
the donor level in the bulk AlGaAs at Ec.
160 CLS
170 E0=8.854D-14
180 Q=1.602D-19
190 INPUT "InGaAs Device?";A$
200 INPUT "Mole fraction of Al";X
210 INPUT "Metal-semiconductor barrier height";VB
220 INPUT "Nd";ND
230 INPUT "Na";NA
240 INPUT "p+ layer thickness";T:T=T*1E-08
250 INPUT "AlGaAs layer thickness";DD:DD=DD*1E-08
260 INPUT "Separation layer thickness in Angstroms";DI:DI=DI
*1E-08
270 COLOR 7
280 E2=E0*(13.2-2.8*X)
290 E1=E0*13.2
300 DEC=.811*X
310 IF A$="Y" OR A$="Y" THEN DEC1=.3 ELSE DEC1=DEC
320 VOFF= DEC-DEC1-Q*ND*DD*DD/(2*E2)+Q*NA*T*T/(2*E1)+VB-Q*ND
*DD*T/E1+EFO
330 IF VOFF > 0 THEN RHS = VOFF + DEC1 ELSE RHS = DEC1
340 DENOM = (DD+DI+E2*T/E1+.0000008)*Q/E2
350 NS = -VOFF/DENOM
360 NS = CINT(1E-09*NS)/1E-09
370 IF VOFF>0 THEN NS=0
380 RHS = RHS-1.25E-13*NS
390 C1=Q*ND*DD*DD/(2*E2)+RHS-Q*NS*(DD+DI)/E2
400 EMAX=0
410 XMAX=0
420 CLS
430 LOCATE 1,1,0
440 GOSUB 830
450 FOR Z=0 TO 180 STEP 18
460 LINE (160,180-Z)-(639,180-Z),6
470 NEXT Z
480 FOR P=160 TO 639 STEP 50*4.79E-06/(DD+DI+T)
490 LINE (P,0)-(P,180),6
500 NEXT P
510 J= -1
520 FOR I=0 TO DI+DD+T+1E-10 STEP 1E-08
530 J=J+1
540 IF I <= DD+DI THEN GOSUB 650

```

```

550 IF I> DD+DI THEN GOSUB 740
560 IF EC > ECMAx THEN GOSUB 790
570 NEXT I
580 LOCATE 9,1,0:PRINT "Ecmax=";ECMAx;
590 PRINT "eV"
600 LOCATE 10,1,0:PRINT "Ns=";NS;
610 PRINT "cm^-2"
620 IF INKEY$ =" " THEN 630 ELSE 640
630 FOR U=1 TO 20:LPRINT:NEXT U
640 END
650 'Routine for Ec and plot for i<dd+di
660 IF I<DI THEN EC=RHS-I*NS*Q/E2 ELSE EC=Q*ND*(I-DI)^2/(2*E
2)+RHS-Q*NS*I/E2
665 IF EC<0 THEN EC=0
670 GOSUB 700
680 IF J=0 THEN LINE (639,180)-(X,Y),7 ELSE LINE -(X,Y),7
690 RETURN
700 'sets value for x and y
710 X=FIX(479*(1-J*1E-08/(DD+DI+T)))+160
720 Y=FIX(180*(1-(EC/2)))
730 RETURN
740 'Routine for Ec and plot for (i>dd+di)
750 EC=C1+Q*ND*DD*(I-DD-DI)/E1-DEC-Q*NA*(I-DD-DI)^2/(2*E1)-Q
*NS*(I-DD-DI)/E1
760 GOSUB 700
770 LINE -(X,Y),7
780 RETURN
790 'Routine for finding Ecmax and xmax
800 ECMAx=EC
810 XMAx=I
820 RETURN
830 'places value on screen
840 LOCATE 2,1,0:PRINT " x=";X
850 LOCATE 3,1,0:PRINT "Vb=";VB;
860 PRINT "V"
870 LOCATE 4,1,0:PRINT "Nd=";ND;
880 PRINT "(cm)^-3"
890 LOCATE 5,1,0:PRINT "Na=";NA;
900 PRINT "(cm)^-3"
910 LOCATE 14,13,0:PRINT "Ec/q"
920 LOCATE 15,10,0:PRINT "(0.2V/div)"
930 LOCATE 6,1,0:PRINT "Voff=";
940 PRINT VOFF;:PRINT "V"
950 LOCATE 7,1,0:PRINT " T=";
960 PRINT T*1E+08;
970 PRINT " ang"
980 LOCATE 8,1,0:PRINT " dd=";
990 PRINT DD*1E+08
1000 PRINT " ang"
1010 LOCATE 9,1,0:PRINT "di=";DI*1E+08;:PRINT "ang"
1020 LOCATE 24,19,0:PRINT "0"
1030 LOCATE 25,21,0:PRINT "0"
1040 LINE (160,180)-(137,190),6
1050 RETURN

```

DEPTH INTO MODFET

(50 ANG/DIV)"

APPENDIX B

University of Illinois Fabrication Procedures



This appendix describes the procedures used to fabricate different MODFET structures from MBE-grown substrates. The substrates were provided by the University of Illinois Coordinated Sciences Laboratory. The procedures begin with indium removal from the back side of the wafer, and conclude with the final overlay metallization step. While the procedure is described for a single sample, it should be understood that several samples from different MBE growths were fabricated at the same time.

#### Cutting

MBE-grown layers are fabricated on large wafers. A small portion of the wafer was scribed off for fabrication. The scribed sample measured approximately  $1 \text{ cm}^2$ . Before processing, the wafer was inspected under a microscope for surface contaminants.

#### Indium Removal

Before MBE growth, indium solder was used to mount the back side of the starting material to a holder. Before FET fabrication, the indium must be removed leaving a smooth surface. A smooth back side is necessary before the wafer can be placed on the spinner for further processing. The following is the sequence of steps used to remove the indium.

1. A solution of  $1 \text{ g HgCl}_2$  in  $10 \text{ ml}$  dimethyl formamide was used. Large quantities of the solution were mixed and stored before this fabrication process.

2. The solution was poured in a small beaker and the wafer immersed in it. Periodically, the beaker was placed in an ultrasonic tank and agitated for 15-20 seconds.
3. The wafer was occasionally removed from the solution and rinsed with methanol from a squeeze bottle. This removed large particles of indium. Before re-immersing in the solution, the wafer was rinsed in deionized water (DIW).
4. After approximately 10 minutes in the solution, all indium was removed from the backside of the wafer. It was again rinsed in methanol, followed by DIW.
5. The wafer was dipped in a solution of Alconox cleaner. This removed any  $\text{HgCl}_2$  that remained on the surface.
6. The wafer was thoroughly rinsed in DIW and dried with dry nitrogen.

#### Lapping

To facilitate handling, a protective coating of photoresist was first placed on the front surface. The back side of the material was then thinned to a thickness of 350-400  $\mu\text{m}$ .

1. The wafer was placed on a glass slide and baked at 110° C for 5 minutes to dry the surface.
2. The wafer was removed from the oven and placed on the photoresist spinner. The wafer was spun and dry nitrogen sprayed on the surface to remove surface particles.
3. Several drops of AZ-1350J photoresist were placed on the wafer's surface. The sample was spun at 5000 rpm for 30 sec.

4. The wafer was again placed on a glass slide and baked at 110° C for 30 minutes. This hardened the photoresist.

5. The wafer was mounted on a lapping block. The block was first heated on a hot plate. Paraffin was melted on the surface and the wafer placed on the block, crystal growth (shiny) side down.

6. Powdered 5  $\mu$ m dry grit was placed on a lapping surface and DIW added to create a slurry mixture. The inverted lapping block was placed on the lapping surface. Using a figure-eight motion with the lapping block, the back surface of the wafer was lapped away. Periodic checks were made with a micrometer until the desired thickness was reached.

7. The wafer was rinsed in DIW to remove lapping grit. It was then removed from the lapping block by reheating the block on a hot plate, melting the paraffin.

8. Paraffin was removed from the wafer with a stream of trichloroethane. The protective photoresist was then removed with an acetone spray. The wafer was cleaned in methanol and DIW, and dried with nitrogen.

#### Mesa Etch

This procedure etched the wafer down to GaAs substrate material, to isolate individual MODFETs.

1. The wafer was dried for 5 minutes at 110° C to remove surface moisture.

2. The wafer was again placed on the photoresist spinner and coated with the AZ 1350 J photoresist. The wafer was spun at 5000 rpm for 30 seconds.

3. The sample was baked at 90° C for 20 minutes.
4. The wafer was aligned under the mesa etch mask and exposed under ultraviolet light (UV) for 6 seconds.
5. The wafer was developed in 5:1, DIW: AZ 351 developer for 45 seconds.
6. The wafer was inspected wafer under the microscope for mesa definition and recycled through the photoresist procedure as necessary.
7. The sample was placed in a beaker of 3:1:1, DIW:H<sub>2</sub>O<sub>2</sub>:HF for 8 seconds. This etched the wafer down to the GaAs buffer layer.
8. The wafer was rinsed thoroughly in DIW to stop the etch.
9. Photoresist was stripped in acetone, cleaned in methanol and DIW, then dried with nitrogen.
10. The resistance of etched areas was measured with probes connected to a curve tracer. A high resistance indicated that the active regions had been completely etched away.

#### Source and Drain Contact

Source and drain ohmic contacts were formed in a two step process. Metal was first evaporated onto the surface. Transient annealing was then used to form the ohmic contacts.

#### Metallization.

1. The wafer was baked at 110° C for 5 minutes to remove surface moisture.
2. AZ 1350 J photoresist was applied and spun for 30 sec-

onds at 5000 rpm.

3. The wafer was softbaked at 90° C for 20 minutes.

4. The photoresist was thickest at the edges of the wafer, and had to be removed there. Black paper cutouts were made just smaller than the sample. The cutouts were placed over the sample in the mask aligner and the edge photoresist exposed to UV. That photoresist was developed in 5:1, DIW:AZ 351 as before.

5. The wafer was placed back in the mask aligner and aligned under the source and drain contact mask. It was exposed for 6 seconds to UV light.

6. The source and drain contact areas were removed in 5:1, DIW:AZ 351.

7. The sample was inspected under the microscope for proper source and drain definition.

8. Sample was loaded into the evaporation chamber, which was then pumped down to approximately  $1 \times 10^{-6}$  torr.

9. Contact metal was evaporated, beginning with 400 Å AuGe. 210 Å of current was applied to the heater. 110 Å Ni was evaporated with the electron gun, using 75 mA gun current. Finally 600 Å Au was applied with 230 Å heater current. Thicknesses were monitored with a Sloan digital thickness monitor.

10. The samples cooled for 10 minutes before the chamber was brought up to atmospheric pressure.

11. Metal was lifted off with an acetone soak. The wafer was periodically placed in an ultrasonic bath for up to 5

seconds to agitate and dissolve the photoresist.

12. Source and drain metal was inspected under a microscope for proper definition.

Source and Drain Alloying to Form Ohmic Contacts.

1. The alloying oven was profiled and stable at 500° C.
2. The sample was placed in a quartz boat and loaded into the sample tube at the end of the oven.
3. The oven was purged with hydrogen for 3 minutes. This time also allowed samples at the end of the sample tube to slowly come up to temperature.
4. A quartz boat with a sample was pushed into the oven and annealed for 50 seconds.
5. The boat was pulled back out to the edge of the tube to cool for 3 minutes.
6. The boat was removed from the oven and the sample from the boat.
7. Finally, the samples were tested on a curve tracer to determine if contacts were ohmic.

Etch p<sup>+</sup>-Layer from Control Samples.

To have control samples without p<sup>+</sup>-layers, the layer under the gate must be removed before applying the gate contact. This step is performed by masking off half of the sample with photoresist (ES samples) and etching under the gate for control samples. The following is the sequence of events for this task.

1. A sample was baked for 5 minutes at 110° C.

2. The sample was placed on a photoresist spinner. Next, AZ 1350 was applied. It was spun at 5000 rpm for 30 seconds.
3. The sample was baked for 20 minutes at 90° C.
4. The sample was placed in a mask aligner. Half of the sample was covered with black paper. That portion covered was designated as the ES sample. The uncovered portion of the sample was exposed to UV.
5. Exposed photoresist was removed in diluted AZ 351 developer. The sample was inspected under a microscope.
6. The sample was placed in a solution of  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{DIW}$  in a concentration of 3:1:150 by volume. Samples were dipped to etch the  $\text{p}^+$ -layer, based on a 30 Å/s etch rate (36).
7. Photoresist was stripped off with acetone and the sample rinsed in methanol and DIW.

#### Apply Gate Contact

With the gate and source contacts applied and alloyed, and with the  $\text{p}^+$ -layer on control samples etched off, the gate Schottky barrier contact was applied.

1. The sample was baked at 110° C for 5 minutes to remove surface moisture.
2. AZ 4110 photoresist was applied and spun for 30 seconds at 5000 rpm.
3. The sample was pre-baked at 70° C for 20 minutes.
4. Photoresist was exposed and developed at the edges of the wafer as before.
5. The wafer was placed in the mask aligner and aligned

under the gate mask. The photoresist was exposed for 7.5 seconds at a power setting of  $8.7 \text{ mW/cm}^2$ .

6. The sample was soaked in chlorobenzene for 15 minutes.

7. The sample was post-baked in a  $90^\circ \text{C}$  oven for 10 minutes.

8. Photoresist was developed for 60 seconds in 3.5:1, AZ 400K developer:DIW.

9. The wafer was soaked for 20 seconds in a "descumming" solution (1:10,  $\text{NH}_4\text{OH}$ :DIW) to remove photoresist from the gate region.

10. The wafer was rinsed in DIW and dried with nitrogen.

11. The wafer was inspected under a microscope for proper gate definition.

12. The sample was placed in an evaporation chamber which was then pumped to approximately  $10^{-6}$  torr.

13. Aluminum or a sequence of titanium and gold was evaporated to form the gate contact. Titanium (500) Å was evaporated with an electron gun at 75 mA, followed by 2000 Å of Au. The heater current was set at 225 A.

14. Samples were cooled for 10 minutes before opening the chamber to atmospheric pressure.

15. The photoresist and metal were lifted off with an acetone soak. The beaker was periodically placed in the ultrasonic tank and agitated for up to 15 seconds. The liftoff process took 10-15 minutes, typically.

16. The sample was rinsed in DIW and dried with nitrogen.



17. The sample was inspected under the microscope for proper gate formation.

18. The sample was tested on the curve tracer for I-V characteristics.

#### Overlay Metal Evaporation

To provide a good surface for bonding, thicker metal was evaporated onto the regions of the contact pads where bond wires would later be attached.

1. The process used here was exactly the same as for gate metallization, with one exception. A different mask was used to allow metallization on source, gate and drain pads, but only in the areas where bond wires were likely to be attached. There is no need to apply thicker metal to the actual gate, between the source and drain contacts.

2. At this point, the samples were ready for post-fabrication DC testing, dicing and mounting, and for microwave testing.

APPENDIX C

Air Force Avionics Laboratory Fabrication Procedures

The fabrication procedures used at the Air Force Avionics Laboratory (AFAL) are similar to those used at UI and described in Appendix B. However, there are significant differences in procedures and equipment used. The process includes indium removal, cleaning, mesa etching, source-drain contact, gate contact, overlay metallization and lapping. The wafers grown at UI by MBE were scribed and a portion of the wafer shipped to AFAL. The samples were approximately 2 cm<sup>2</sup>.

#### Indium Removal.

Before processing could proceed, the indium used to hold the wafer in place in the MBE system was removed. This was accomplished by mounting a Si wafer on top of the MODFET wafer and etching the indium in hot HCl.

1. The MODFET chip, along with a clean, bare Si wafer were baked at 150° C for 60 minutes to remove surface moisture.
2. Hexamethyldisilazene (HMDS) was dropped onto the MODFET wafer to promote surface adhesion. After 10 seconds, the wafer was spun at 1000 rpm for 30 seconds. After another 10 seconds, the wafer was coated with MP-1375 photoresist and spun again for 30 seconds.
3. The same procedure was performed on the bare Si wafer.
4. The MODFET wafer was placed upside down on the surface of the Si wafer.
5. The Si/MODFET structure was baked at 100° C for 45 minutes.
6. A beaker of HCl was heated on a hot plate to 65° C.

7. The layered wafers were placed in the warm HCl. The indium was etched from the backside of the MODFET wafer, while the front of the wafer was protected by photoresist and the Si wafer. The etch continued until no more surface reaction (bubbling) was observed.
8. The wafers were placed in a beaker of DIW to stop the reaction.. The wafers were then rinsed in flowing DIW until the water reached 10 M $\Omega$ .
9. The wafers were blown dry with nitrogen.
10. The wafers were soaked in acetone overnight. They were then separated carefully.
11. The MODFET wafer was cleaned by rinsing in trichloroethane (TCE), acetone, methanol and isopropyl alcohol. It was again dried with nitrogen.

#### Mesa Etch

1. The wafer was inspected under a microscope for surface contaminants. When needed, wafers were cleaned again with TCE, acetone, methanol and isopropyl alcohol.
2. The MODFET wafer was baked at 150° C for 60 minutes.
3. HMDS was dropped on the wafer. After 10 seconds, the wafer was spun at 4000 rpm for 30 seconds. MP-1470 photoresist was applied and spun at 4000 rpm for 30 seconds.
4. The wafer was softbaked at 90° C for 30 minutes.
5. The coated wafer was exposed under the mesa etch mask for 20 seconds.
6. The photoresist was developed for 60 seconds with MP 351

developer diluted 1:5 with DIW. To develop, the wafer was placed on a spinner, spun at low speed and the diluted developer applied continuously with a spray bottle.

7. The resist was hard baked for 30 minutes at 100° C.

8. The wafer was placed in 8:1:1, DIW:H<sub>2</sub>O<sub>2</sub>:HF for 20 seconds. It was rinsed in flowing DIW to 10 MΩ, then blow-dried with nitrogen.

9. The mesa height was measured with a DEKTAC profilometer. Mesa height was typically 2000-3000 Å.

#### Source and Drain Contacts Application

As with the UI procedure, source-drain ohmic contacts were formed by evaporating metal onto the surface and alloying in a furnace.

#### Metallization.

1. The wafer was baked at 150° C for 60 minutes.

2. HMDS was applied to the wafer. After 10 seconds, the wafer was spun at 4000 rpm for 30 seconds. MP1400-17 photoresist was applied and spun at 4000 rpm for 30 seconds.

3. The coated wafer was softbaked for 30 minutes at 90° C.

4. The wafer was aligned and exposed under the source-drain contact mask for 25 seconds.

5. The wafer was soaked exactly 2 minutes in clean chlorobenzene. It was immediately dried with nitrogen.

6. The wafer was post baked at 90° C for 30 minutes.

7. Photoresist was developed as before with 351 developer for 60 seconds.

8. The wafer was dipped in 20:1, DIW:HCl for 20 seconds, then rinsed in DIW to 10 M $\Omega$ .
9. The sample was loaded into the evaporation chamber. The chamber was pumped down to approximately  $10^{-6}$  torr.
10. Contact metal was evaporated. The evaporation consisted of 50 Å Ni, 170 Å Ge, 330 Å Au, 150 Å Ni, and 2000 Å Au.
11. An acetone soak was used to dissolve photoresist and lift off excess metal. After 10-15 minutes in the soak, acetone from a spray bottle was squirted over the wafer completely remove photoresist and to drive away unwanted metal.
12. The wafer was rinsed in clean acetone, methanol and isopropyl alcohol.

#### Alloying.

1. The wafer was placed in the rapid transient alloying oven.
2. The computer-controlled oven was heated to 425° C for approximately 5 seconds. The temperature was lowered to 400° C for 45 seconds.
3. The wafer was removed from the oven and DC tests were performed to evaluate the ohmic contacts. A current versus voltage curve was recorded between source and drain contacts, and TLM measurements were made.

#### Gate Contact Application and Control Sample Etch

1. The wafer was baked at 150° C for 60 minutes.
2. HMDS was applied. After 10 seconds, the wafer was spun

at 4000 rpm for 30 seconds. MP1400-17 photoresist was applied and spun at 4000 rpm for 30 seconds.

3. Wafer was softbaked at 90° C for 30 minutes.

4. The wafer was aligned under the gate contact mask and exposed for 25 seconds.

5. The wafer was soaked in chlorobenzene for 2 minutes, then dried with nitrogen.

6. The wafer was post-baked at 90° C for 15 minutes.

7. The wafer was developed in 5:1 DIW:351 developer for 60 seconds.

8. The sample was cleaved into two pieces. One half was designated the control sample (part A) and the other the ES device (part B).

9. The control sample was dipped in pH 7.05 etch for 5-7 seconds, depending on the thickness of the grown  $p^+$ -layer thickness. The ES device was not etched.

10. The sample was placed in the evaporation chamber. The chamber was pumped down to  $10^{-6}$  torr. Metal was evaporated with the electron gun. First, 250 Å Cr was evaporated, followed by 750 Å Pd and 2000 Å Au.

11. The wafer was soaked in acetone for 10 minutes. Photoresist was dissolved and excess metal was removed with acetone from a squirt bottle.

12. The wafer was cleaned with acetone, methanol and isopropyl alcohol.

13. DC characteristics were measured on the semiconductor parameter analyzer.

### Overlay Metal Evaporation

Overlay metal was evaporated onto the wafer to provide thick surfaces for bonding. The procedure was again the same as for gate metallization, without control sample etching. An overlay mask was used.

### Etching of $p^+$ -Layer Between Contacts

With the devices completely fabricated, the  $p^+$  layer was etched from between source, gate and drain contacts. This was performed on both control and ES samples, since both still had the  $p^+$ -layer present. Since the control sample was etched through the gate mask, there was p-doped material between contacts that needed to be removed. To remove the layer, source, gate and drain contacts were used as a mask. The etchant was applied to remove the layer between contacts. Again, pH 7.05 etchant was applied for 5-7 seconds. Because of the small distance between contacts (1-2  $\mu\text{m}$ ), it was necessary to perform the etch in an ultrasonic bath. This bath ensured that the etchant would easily wet the channel between contacts.



APPENDIX D

Plotted Microwave Data

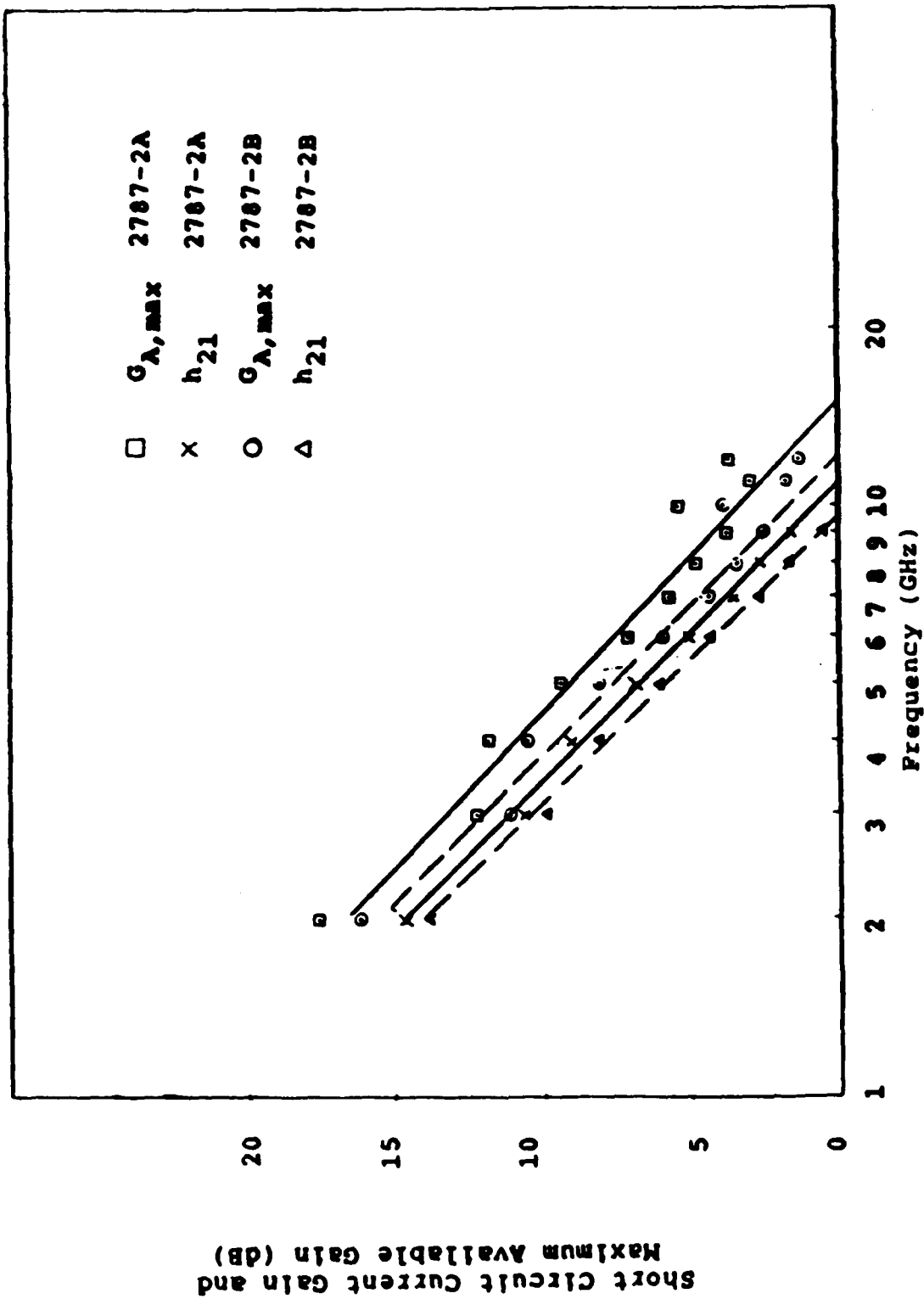


Figure 38. Plotted Values of  $G_{A,max}$  and  $h_{21}$  for Device 2787-2. Lines are Fit to the Data to Give  $G_{A,max}$  and  $h_{21}$  Values at the x-Intercepts.

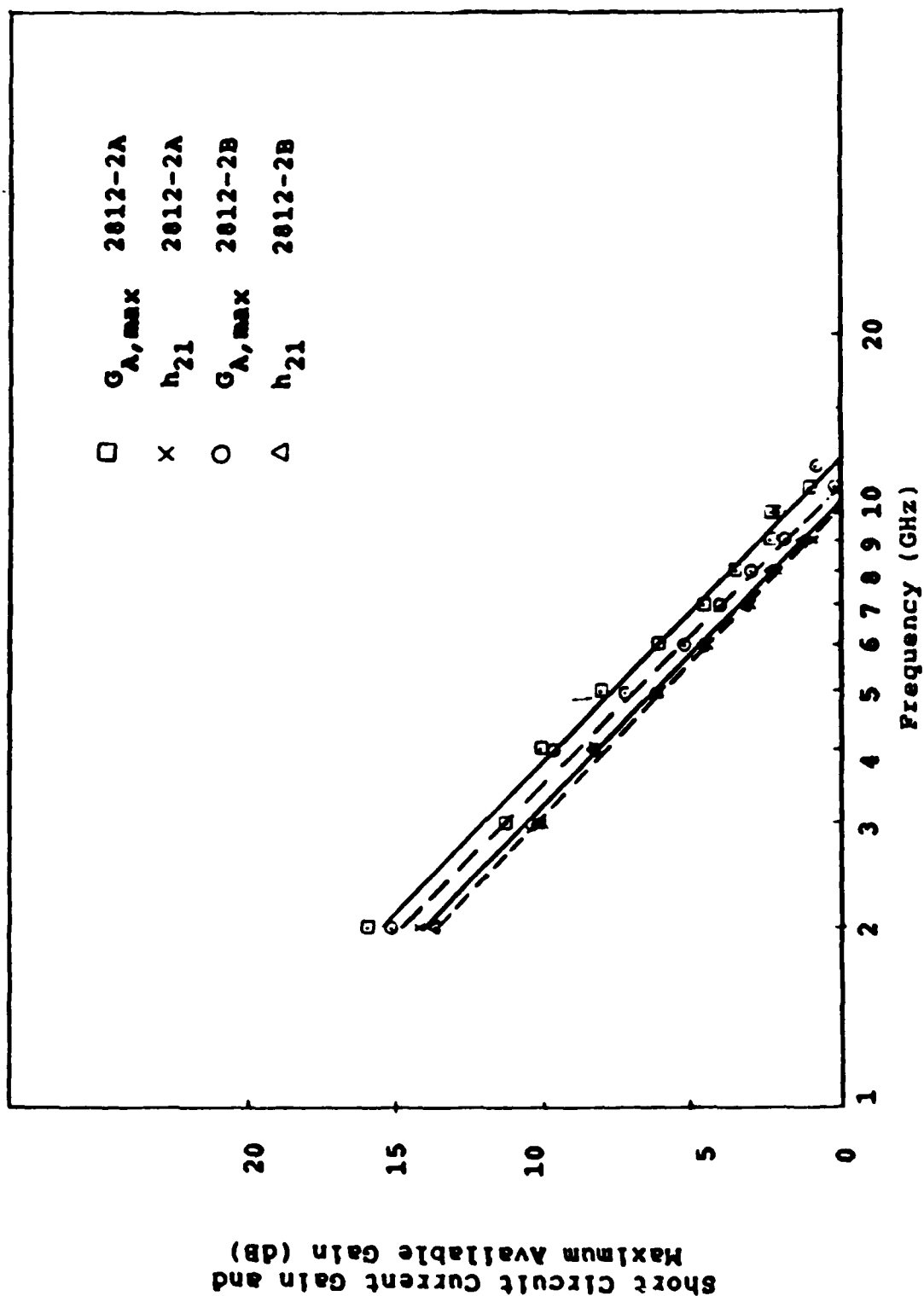


Figure 39. Plotted Values of  $G_{A,max}$  and  $h_{21}$  for Device 2812-2. Lines are Fit to the Data to Give  $G_{A,max}$  and  $h_{21}$  Values at the x-Intercepts.

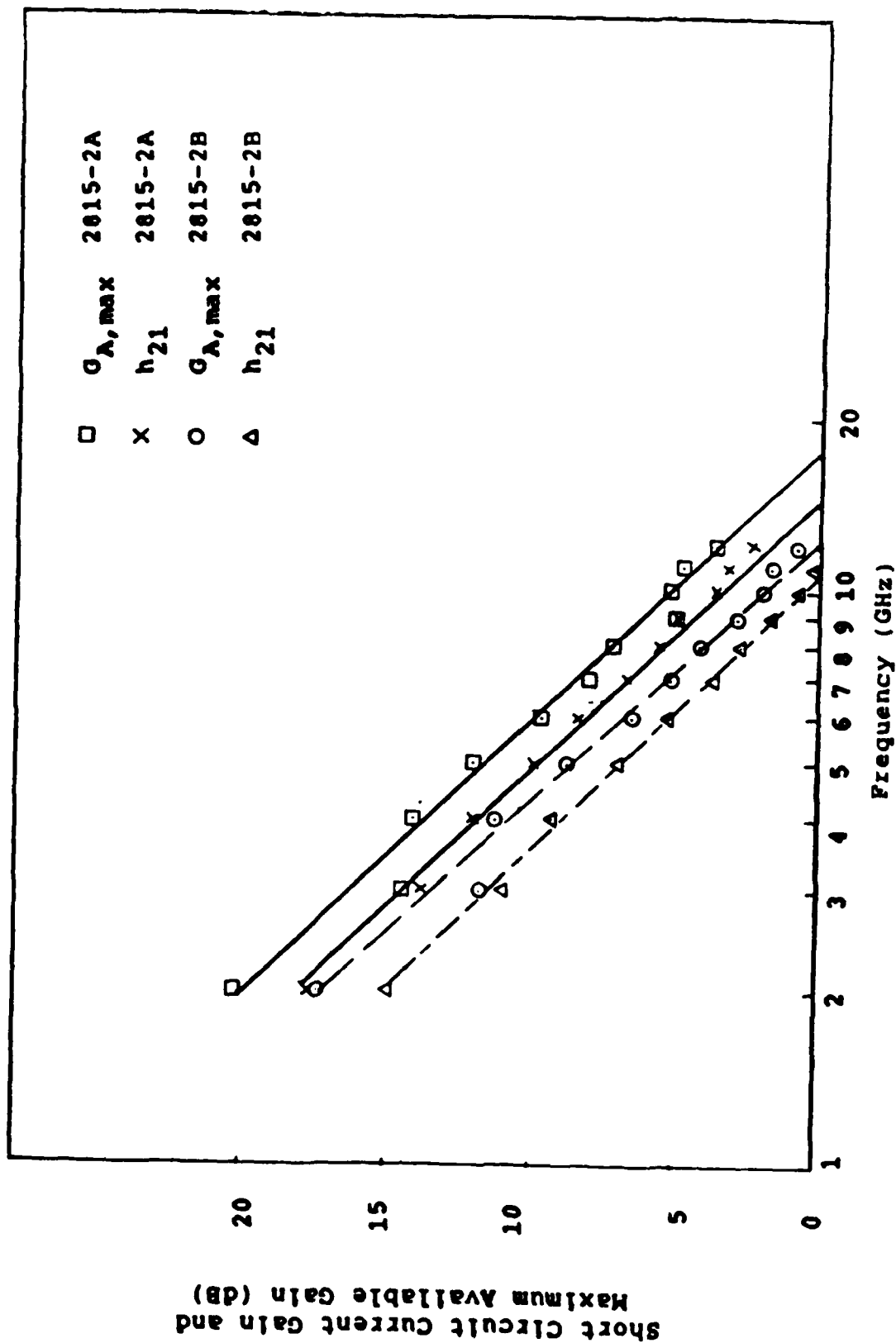


Figure 40. Plotted Values of  $G_{A,max}$  and  $h_{21}$  for Device 2815-2. Lines are Fit to the Data to Give  $f_{T,max}$  and  $f_T$  Values at the x-Intercepts.

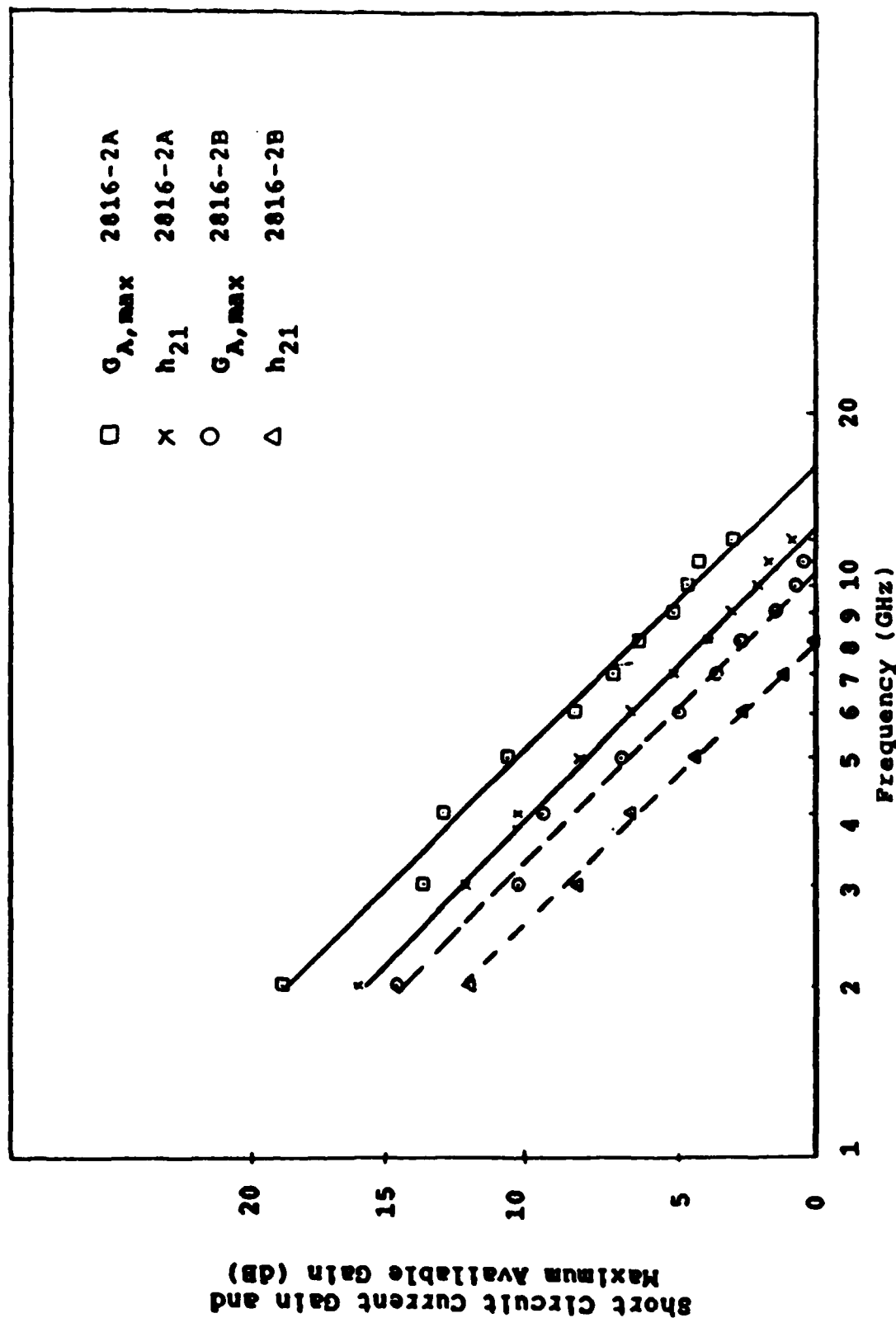


Figure 41. Plotted values of  $G_{A,max}$  and  $h_{21}$  for Device 2816-2. Lines are fit to the Data to  $G_{A,max}$  and  $h_{21}$  Values at the x-Intercepts.

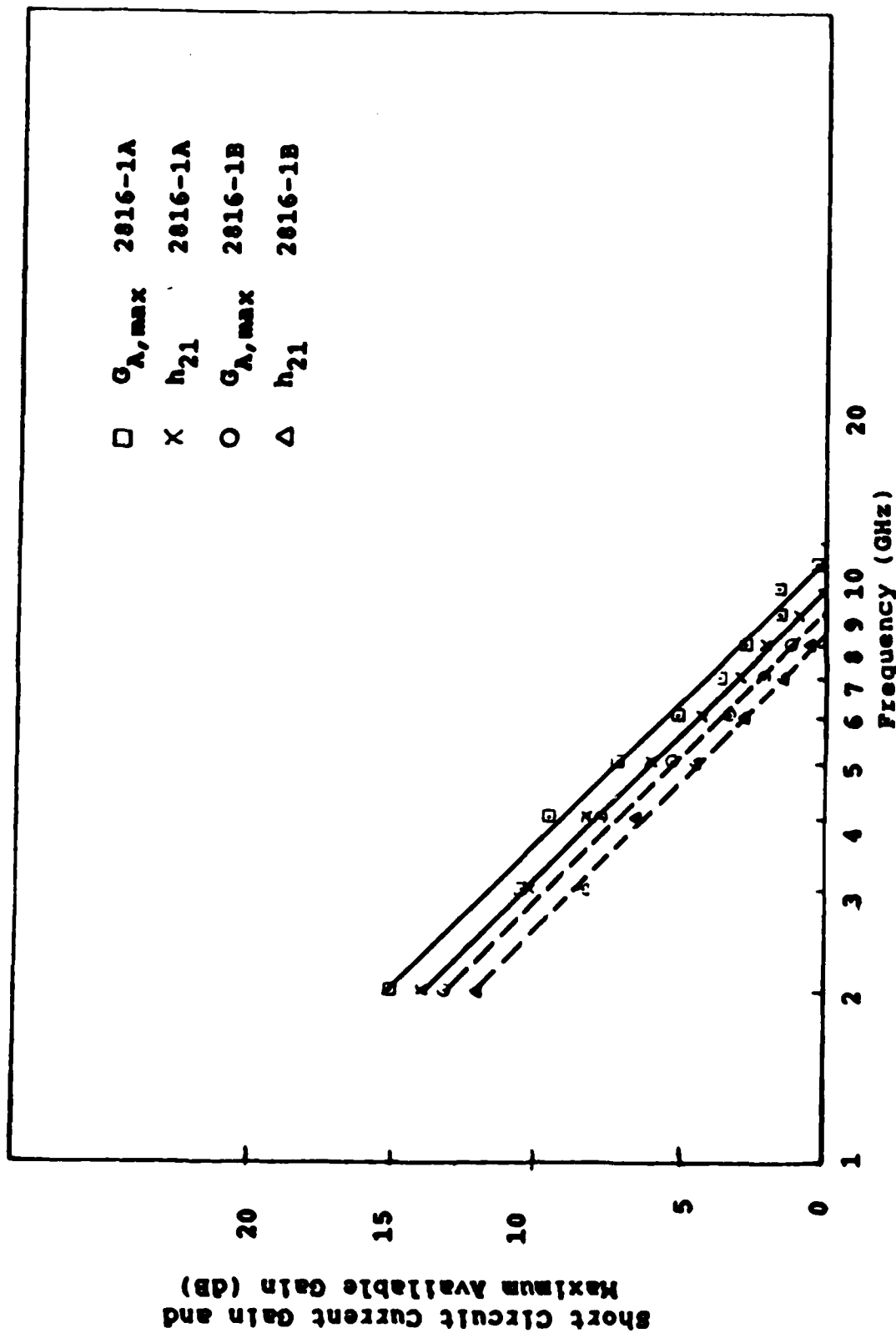


Figure 42. Plotted Values of  $G_{A,max}$  and  $h_{21}$  for Device 2816-1. Lines are Fit to the Data to  $G_{A,max}$  and  $h_{21}$  Values at the x-Intercepts.

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## VITA

Lieutenant Thomas E. McLaughlin was born on December 13, 1956 in Wooster, Ohio. He graduated from Coronado High School in Colorado Springs, Colorado in 1974. He entered the Air Force in 1975, and served for nearly four years. He was discharged in 1979 with an Air Force ROTC scholarship and attended the University of Nebraska-Lincoln. While there, he served as a laboratory technician at the Nebraska Engineering Center, working in semiconductor thin-film growth technology. In December 1982, he was awarded the degree of Bachelor of Science in Electrical Engineering (distinction). At graduation, he was commissioned as an ROTC honor graduate in the Air Force. He was assigned to the Air Force Weapons Laboratory, Kirtland AFB NM in January 1983, where he served as a staff research engineer. He performed and directed research on the effects of Nuclear Electromagnetic Pulse phenomena on aircraft electronics and subsystems, as well as the methods of limiting those effects. He then entered the School of Engineering, Air Force Institute of Technology, in May 1985.

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*thesis*

In this investigation, modulation doped field-effect transistors (MODFETs) were fabricated. Two recently developed improvements to the MODFET structure were incorporated to produce an electronic device that had never before been fabricated. Highly p-doped surface layers were incorporated under the gate contact of the device. These layers have been shown to increase the Schottky barrier height at the gate contact on devices known as enhanced Schottky (ES) MODFETs. Pseudomorphic AlGaAs/InGaAs technology was also incorporated for its proven unsurpassed electron saturation velocity and resulting high speed of operation. Those two complementary technologies were combined in this effort to take advantage of fast speed of operation and high Schottky barrier heights.

To evaluate the response of these ES pseudomorphic devices, their characteristics were measured and compared directly with those of reference samples fabricated at the same time from the same substrate material. The p-layers of the reference transistors were etched off chemically just before deposition of gate contact metal. The peak transconductance, threshold voltage, contact resistance and barrier height of all devices were measured at direct current (DC). Also, microwave S-parameters were measured over the range of 2 to 12 gigahertz (GHz).

Qualitatively, the performance of devices fabricated in this effort approached the best reported for devices of this family. These devices exhibited transconductance as high as 230 mS/mm. This value is unsurpassed for devices with the 1.35 - 1.5  $\mu\text{m}$  gate lengths used here. Similarly, the devices were capable of providing gain at frequencies as high as 17.5 GHz. Normalized contact resistances were also measured. The lowest value observed here (0.002  $\Omega\text{-mm}$ ) surpasses the best published value of 0.035  $\Omega\text{-mm}$  for MODFET devices.

Based on calculations using a charge control model developed in an earlier effort, the devices with p-type layers were expected to exhibit higher gate Schottky barrier heights than similar reference samples without p-layers. Unexpectedly, there was no evidence of the enhanced barrier height. Those devices exhibited Schottky barrier heights consistently slightly lower than those of the reference transistors without p-layers, fabricated from the same substrate material. Three different physical phenomena are given as possible explanations for this observation.

The reference transistors similarly exhibited higher transconductance, threshold voltage and microwave response than the samples with p-layers. This observation can be traced to the greater distance between the gate contact and the current conduction channel in the device with the p-layer.

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